

SHARP SERVICE MANUAL



CODE: 00ZERA450SVSM

ELECTRONIC CASH REGISTER

MODEL ER-A450S

SRV Key : LKGIM7113RCZZ
PRINTER: PR-45M

("V" version)

CAUTION

EXTREME CAUTION MUST BE TAKEN WHEN SERVICING THIS MACHINE. EVEN THOUGH THE MODE SWITCH IS IN THE OFF POSITION, VOLTAGE IS STILL SUPPLIED TO THE ENTIRE MACHINE.

WHEN WORKING ON THIS MACHINE MAKE SURE THAT THE POWER CORD IS REMOVED FROM THE WALL OUTLET.

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PARTS GUIDE

Parts marked with "▲" are important for maintaining the safety of the set. Be sure to replace these parts with specified ones for maintaining the safety and performance of the set.

CHAPTER 1. SPECIFICATIONS

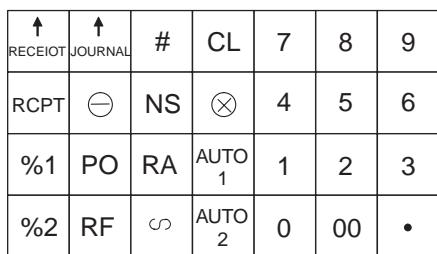
1. Appearance/Rating

1) Rating

Power source	Official voltage and frequency
Power consumption	Standby: 11.5 W Maximum: 42 W (max.)
Operating temperature	0°C ~ 40°C
Operating humidity	10% ~ 90% (RH)
Physical dimensions, including the drawer	355(W) × 424(D) × 308(H)mm
Weight	13.5 kg

2. Keyboard

1) Standard keyboard layout



PLU/ SUB	EAN	AMT	INQ	VAT	CASH#
5	10	15	20	EX1	EX2
4	9	14	19	CR1	CR2
3	8	13	18	CH1	CH2
2	7	12	17	ST	
1	6	11	16		TL

Fig. 2-1

2) Key top name

① Standard Key Top

KEY TOP	DESCRIPTION
0 to 9, 00	Numeric keys
•	Decimal point key
CL	Clear key
⊗	Multiplication key
1 to 20	Department keys
↑ RECEIPT	Receipt paper feed key
↑ JOURNAL	Journal paper feed key
RCPT	Receipt print and Receipt on/off key
%1, %2	Percent keys
⊖	Discount key
PO	Paid out key
RF	Refund key
#	Non-add code entry key
NS	No sale key
RA	Received on account key
⊖	Void key
AUTO1, AUTO2	Automatically entry keys
PLU/SUB	PLU/Subdepartment code entry key
AMT	Amount entry key
VAT	Value added tax key
EX1, EX2	Foreign currency exchange keys
CASH#	Cashier code entry key
CR1, CR2	Credit keys
CH1, CH2	Check keys
EAN	EAN code entry key
INQ	EAN preset amount inquiry key

KEY TOP	DESCRIPTION
ST	Subtotal key
TL	Total (Cash eoeal) key

② Optional Key Top

KEY TOP	DESCRIPTION
21 to 50	Department 21 to 50 key
GC COPY	Guest check copy key
%3, %4	Percent keys
⊖2, ⊖3, ⊖4	Discount key
AUTO3 ~ AUTO10	Automatically entry keys
CA2	Cash total 2 key
CH3, CH4	Check keys
CR3, CR4	Credit key
EX3, EX4	Foreign currency exchange keys
RA2	Received on account key
PO2	Paid out key
1/2	1/2 key
VAT SHIFT	Value added taxshift key
DIFFER ST	Difference subtotal key
CLK #	Clerk code entry key
DEPT#	Department code entry key
NO DEL	EAN non delete key
PRCHNG	EAN price change key
REPEAT	EAN repeat entry key
000	"000" key
1 to 68	Direct PLU/SUB department keys

3. Mode switch

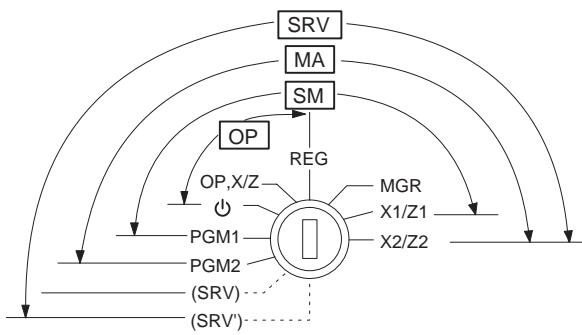


Fig. 3-1

- * The key can be removed in the REG or OFF position.
- * In the SRV' mode, key inputs are prohibited and no display is made.

[Functions]

- Function for each key position
- SRV': System reset
- SRV: Service mode (Service programming)
- PGM2: Allows programming of an item that is not changed frequently, in addition to the PGM1 mode programming.
- PGM1: Allows programming of items frequently changed (e.g. department, PLU pricing, and discount rate setting).
- OP, X/Z: Allows X or Z operation by clerks or cashiers.
- REG: Allows registrations.
- MGR: Allows the operations, by authorized person such as a manager (e.g. correction after transaction finished or cancellation of entry limits), which are not permitted to ordinary cashiers.
- X1/Z1: Allows reading and resetting of a day's sales total.
- X2/Z2: Allows reading or resetting sales totals in a specified period.
- ⏻: Switching off the display to prevent key board entries.

4. Display

1) Layout

① Operator display

1.2.3.4.5.6.7.8.9.0.

Fig. 4-1

	7 segment display (LED)
No. of positions	10
Color of display	Yellow Green
Character size	14.2 (H) × 8.0 (W) mm

② Customer display (Pop-up display)

1.2.3.4.5.6.7.

Fig. 4-2

	7 segment display (LED)
No. of positions	7
Color of display	Yellow Green
Character size	14.2 (H) × 8.0 (W) mm

Display contents

<Segment>

	Display Position	Description
Amount	1-8	
Minus sign	4-10	-: Floating
Error	10	E
PGM Mode	10	P
VOID Mode	10	u
TL, CH, CR	10	F: Lights up when a registration is finalized by depressing TL, CH, CR key
SUB TOTAL/short tender	10	o
Change	10	C: Light up whenever the change due amount appears in the display.
Foreign currency sub total	10	c
Department	9-10	No zero-suppressed
PLU	5-10	No zero-suppressed
Repeat	8	Endless count, starting from 2.
Receipt OFF	9	_
Cashier No.	2-3	-xx-: cashier code
Clerk No.	2-3	C-xx-: clerk code
CCD	10	C: Light up when CCD is compulsory.
compulsory		

<Decimal point>

	Display Position	Description
Decimal point	4-1	
TAB	4-1	
Sentinel	10	
VAT shift	8	

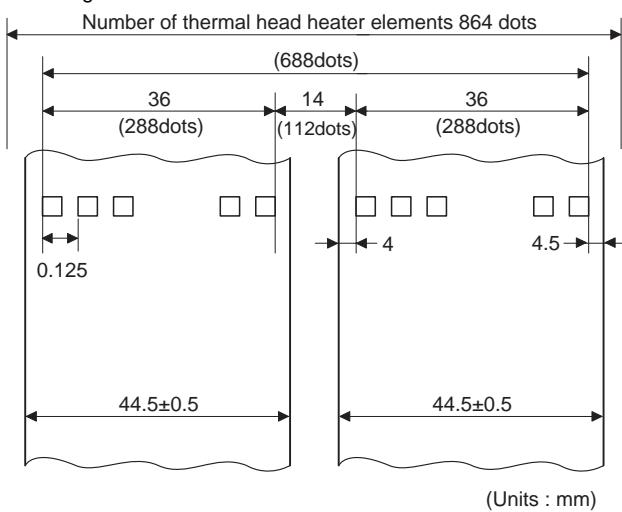
5. Specifications

1) Printer (PR-45M)

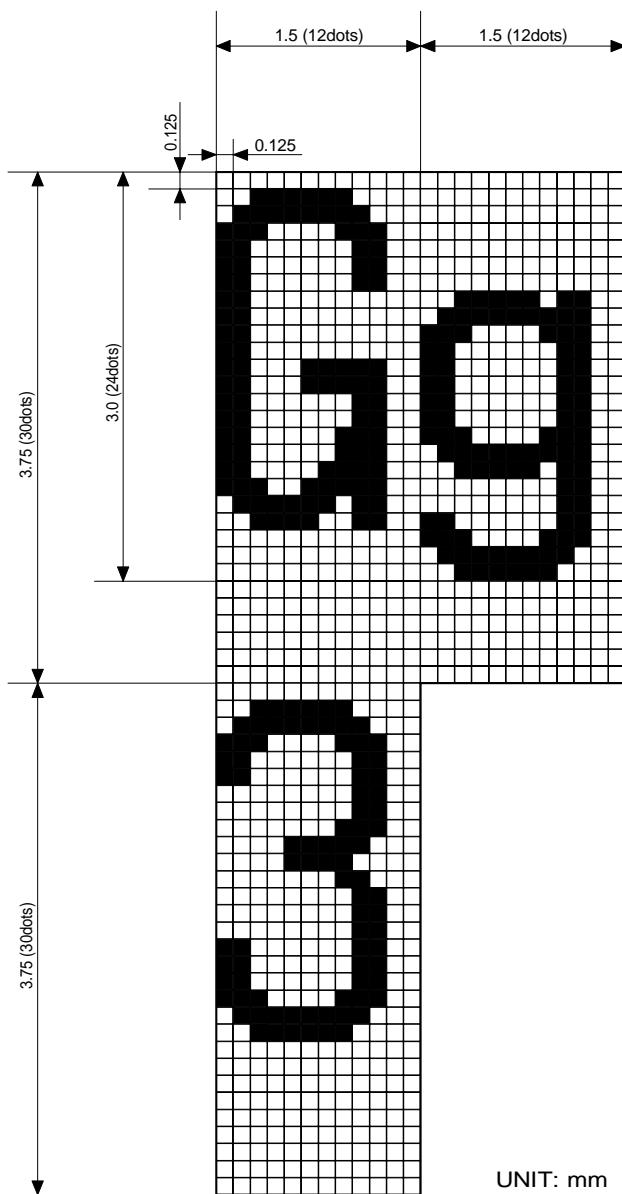
- No. of station: 2: Receipt and Journal
- Validation: No
- Printing system: Line thermal
- No. of dot: Receipt: 288 dots
Journal: 288 dots
- Dot pitch: Horizontal: 0.125 mm
Vertical: 0.125 mm
- Font: 10 dots (W) × 24 dots (H)
- Printing capacity: Receipt: Max. 24 characters
Journal: Max. 24 characters
- Character size: 1.25 mm (W) × 3.0 mm (H):
At 10 × 24 dots
- Print pitch: Column distance: 1.5 mm
Row distance: 3.75 mm
- Print speed: Approximate 50 mm/s (13.3 lines/sec)
- Paper feed speed (Manual feed): Approximate 40 mm/s
- Reliability: Mechanism MCBF 5 million lines
Head life 5 × 10⁷ pulses
- Paper end sensor: Yes (Receipt and Journal)

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- Cutter: Manual
- Paper near end sensor: No
- Printing area:



- Print format:



- Option:

For PR-58M: ER-01AC (Auto cutter unit)

2) Paper

Item	Description
Name	Heat-quality paper
Roll dimension	44.5 ± 0.5 mm in width
Thickness	0.06 mm to 0.08 mm

3) Cutter

- Method: Manual

6. Drawer

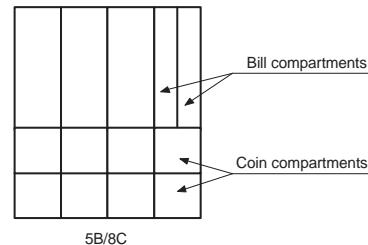
1) Specification

(1) Drawer box and drawer

Model name	SK-420
Size	355 (W) × 424 (L: included lock key) × 120 (H: included rubber leg)
Color	GRAY 368
Material	Metal
Bell	—
Release lever	Standard equipment; Situated at the bottom
Drawer open sensor	Standard equipment

2) Money case

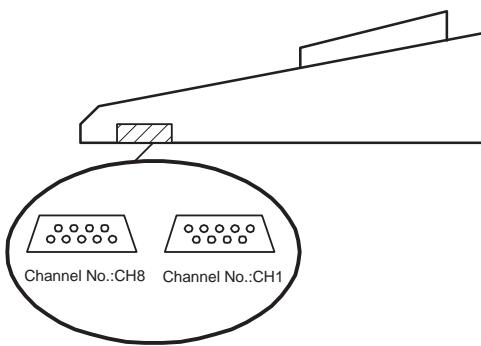
Separation from the drawer	Allowed
Separation of the coin compartments from the money case	Allowed
Bill separator	—
Number of compartments	5B/8C



3) Lock

Location of the lock	Front	
Method of locking and unlocking	Locking:	Insert the drawer lock key into the lock and turn it 90 degrees counterclockwise.
	Unlocking:	Insert the drawer lock key into the lock and turn it 90 degrees clockwise.
Key No.	SK1-1	

7. RS232 Interface



NOTE:

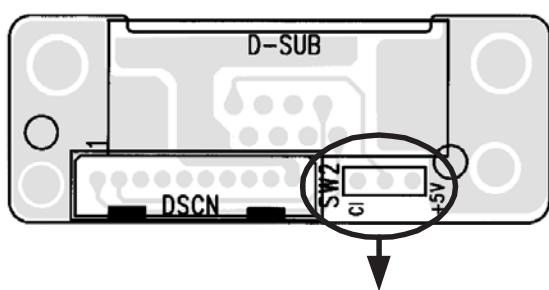
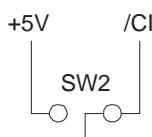
Optional bar code reader: When connecting an ER-A6HS1, connect it to the CH8 and switch the No.9 pin signal to the +5V signal.
When connecting other RS232 device to the CH8, make sure the No.9 pin signal is proper before connecting the device.

1) Channel No. : CH1

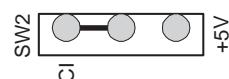
1	/CD
2	RD
3	SD
4	/ER
5	GND
6	/DR
7	/RS
8	/CS
9	/CI

2) Channel No. : CH8

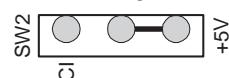
1	/CD
2	RD
3	SD
4	/ER
5	GND
6	/DR
7	/RS
8	/CS
9	/CI



Pin No.9 : /CI signal (Default)



Pin No.9 : +5V signal



The No.9 pin signal of the CH8 can be selected between the /CI signal and the +5V signal by changing the connection of the SW2 (initial value: /CI signal)



ER-A450S

CHAPTER 2. OPTIONS

1. System configuration

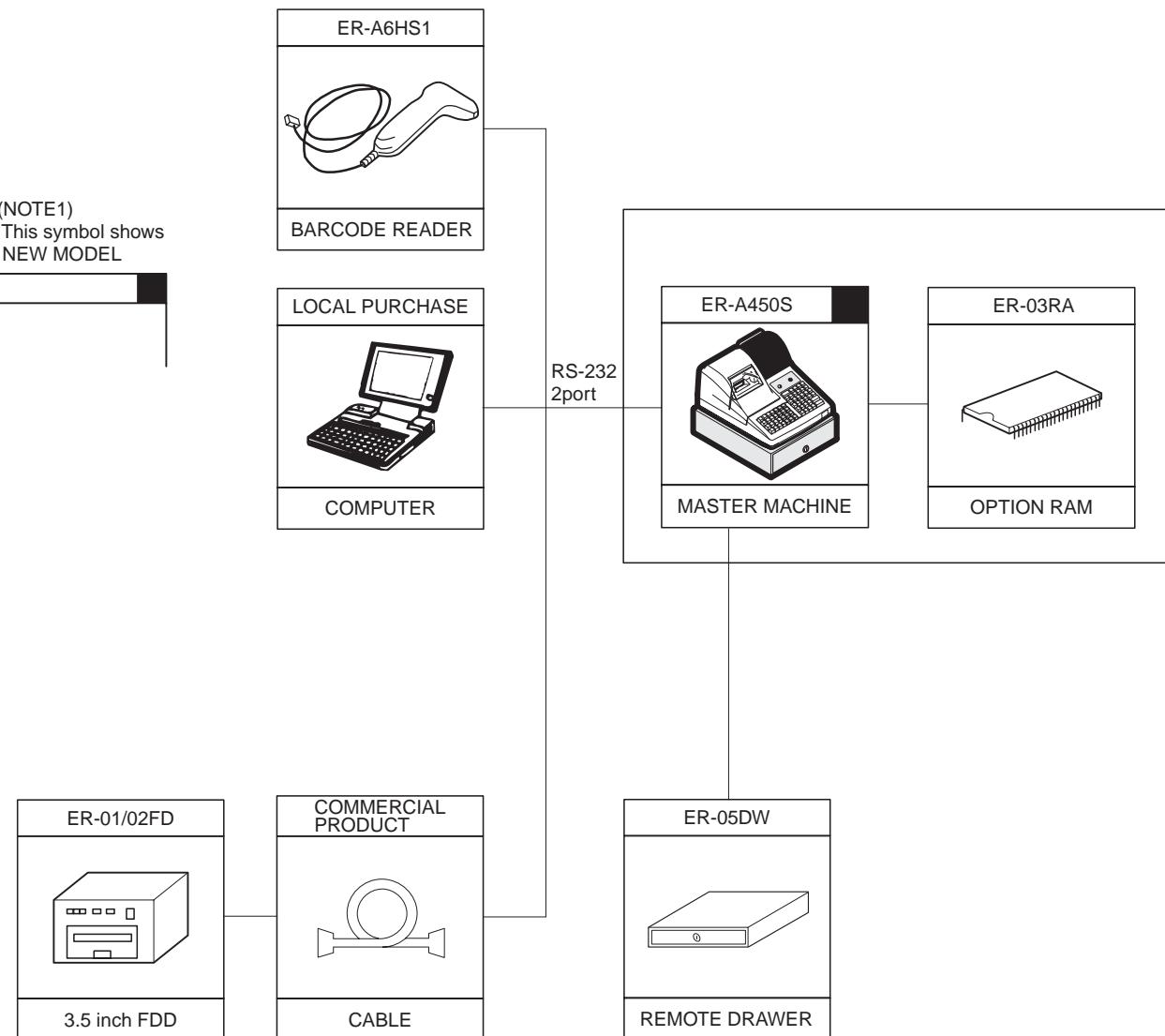


Fig. 1-1

2. Options

No.	NAME	MODEL	DESCRIPTION
1	EXPANSION RAM CHIP	ER-03RA	512K bytes RAM CHIP
2	REMOTE DRAWER	ER-05DW	
3	PRESETS LOADER	ER-01FD/02FD	FD unit
4	KEY TOP KIT	ER-11KT7	1 × 1 KYE TOP UNIT
		ER-12KT7	1 × 2 KYE TOP UNIT
		ER-22KT7	2 × 2 KYE TOP UNIT
		ER-11DK7G	1 × 1 DUMMY KYE KIT
		ER-51DK7G	5 × 1 DUMMY KYE KIT
5	COIN CASE	ER-58CC	5B/8C
6	COIN CASE COVER	ER-03CV	5B/8C
7	BARCODE READER	ER-A6HS1	

3. Service options

No.	NAME	PARTS CODE	PRICE RANK	DESCRIPTION
1	SERVICE KEY	LKGIM7113RCZZ	AF	
2	MODE KEY GRIP COVER	LKGIM7126BHZZ	AL	OP key only
3	DRIP-PROOF KEYBOARD COVER	GCÖVH7126BHZZ	BE	Include the switch cover
4	JOURNAL NEAR END SENSOR UNIT	DUNTK3677BH03	BB	Q'ty: 1
	Screw (Sensor unit – Top cabinet)	XEBSD30P08000	AA	Q'ty: 1
	Screw (Sensor unit – Earth wire – Top cabinet)	XHBSD30P04000	AA	Q'ty: 1
	Screw (Earth wire – Top cabinet)	LX-BZ6778BHZZ	AA	Q'ty: 1
	Earth wire	QCNW-7895BHZZ	AF	Q'ty: 1
	Connector (2pin)	QCNCM6865RC0B	AA	Q'ty: 1
5	TEXT PRESET KEYBOARD COVER	GCÖVB7153BHZZ	BH	
6	ONE HOLE CASHIER KEY KIT	DKIT-8669BHZZ	—	

4. Service tools

No.	NAME	PARTS CODE	PRICE RANK	DESCRIPTION
1	RS-232 LOOP BACK CONNECTOR	UKÖG-6705RCZZ	BU	
2	KEY TOP REMOVER	UKÖG-6634RCZZ	AX	
3	2 × 2 KEY TOP INSTALLING JIG	UKÖG-6725BHZZ	BP	

5. Supplies

No.	NAME	PARTS CODE	PRICE RANK	DESCRIPTION
1	ROLL PAPER	TPAPR6645RC05	AY	5 roll/pack

CHAPTER 3. SRV. RESET AND MASTER RESET

1. SRV. reset (Program Loop Reset)

Used to return the machine back to its operational state after a lock-up has occurred.

Procedure

- Method 1
 - Unplug the AC cord from the wall outlet.
 - Set the mode switch to (SRV') position.
 - Plug in the AC cord to the wall outlet.
 - Turn to (SRV) position from (SRV') position.

- Method 2

- 1) Set the mode switch to PGM2 position.
 - 2) Turn off the AC switch.
 - 3) While holding down JOURNAL FEED key and RECEIPT FEED key, Turn on the AC switch.

Note: When disassembling and reassembling always power up using method 1 only. Method 2 will not reset the CKDC8.

Note: SRV programming job#926-B must be set to "4" to allow PGM program loop reset.

2. Master reset (All memory clear)

There are two possible methods to perform a master reset.

- MRS-1

Used to clear all memory contents and return machine back to its initial settings and return keyboard back to default keyboard layout.

Procedure

- 1) Unplug the AC cord from the wall outlet.
 - 2) Set the MODE switch to the (SRV') position.
 - 3) Plug in the AC cord to the wall outlet.
 - 4) While holding down JOURNAL FEED key, turn to (SRV) position from (SRV') position.

- MRS-2

Used to clear all memory and keyboard contents.

This reset returns all programming back to defaults. The keyboard must be entered by hand.

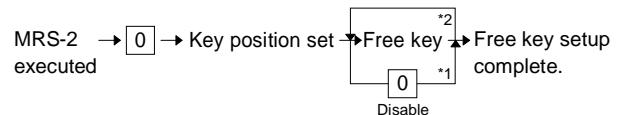
This reset is used if an application needs different keyboard layout other than that supplied by a normal MRS-1.

Procedure

- 1) Unplug the AC cord from the wall outlet.
 - 2) Set the MODE switch to the (SRV') position.
 - 3) Plug in the AC cord to the wall outlet.
 - 4) While holding down JOURNAL FEED key and RECEIPT FEED key, turn to (SRV) position from (SRV') position.

* After the execution of MRS-2, only the RECEIPT FEED and JOURNAL FEED keys can remain effective on key assignment. Any key can be assigned on any key position on the main keyboard.

[key setup procedure]



NOTES:

*1: When the 0 key is pressed, the key of the key number on display is disabled.

*2: Push the key on the position to be assigned. With this, the key of the key number on display is assigned to that key position.

Key number	Key name	Key number	Key name
1	Numeric key "0"	10	Numeric key "9"
2	Numeric key "1"	11	Numeric key "00"
3	Numeric key "2"	12	Numeric key "000"
4	Numeric key "3"	13	Decimal point key
5	Numeric key "4"	14	CL key
6	Numeric key "5"	15	⊗ key
7	Numeric key "6"	16	ST key
8	Numeric key "7"	17	TL key
9	Numeric key "8"		

CHAPTER 4. HARDWARE DESCRIPTION

1. Hard ware block diagram

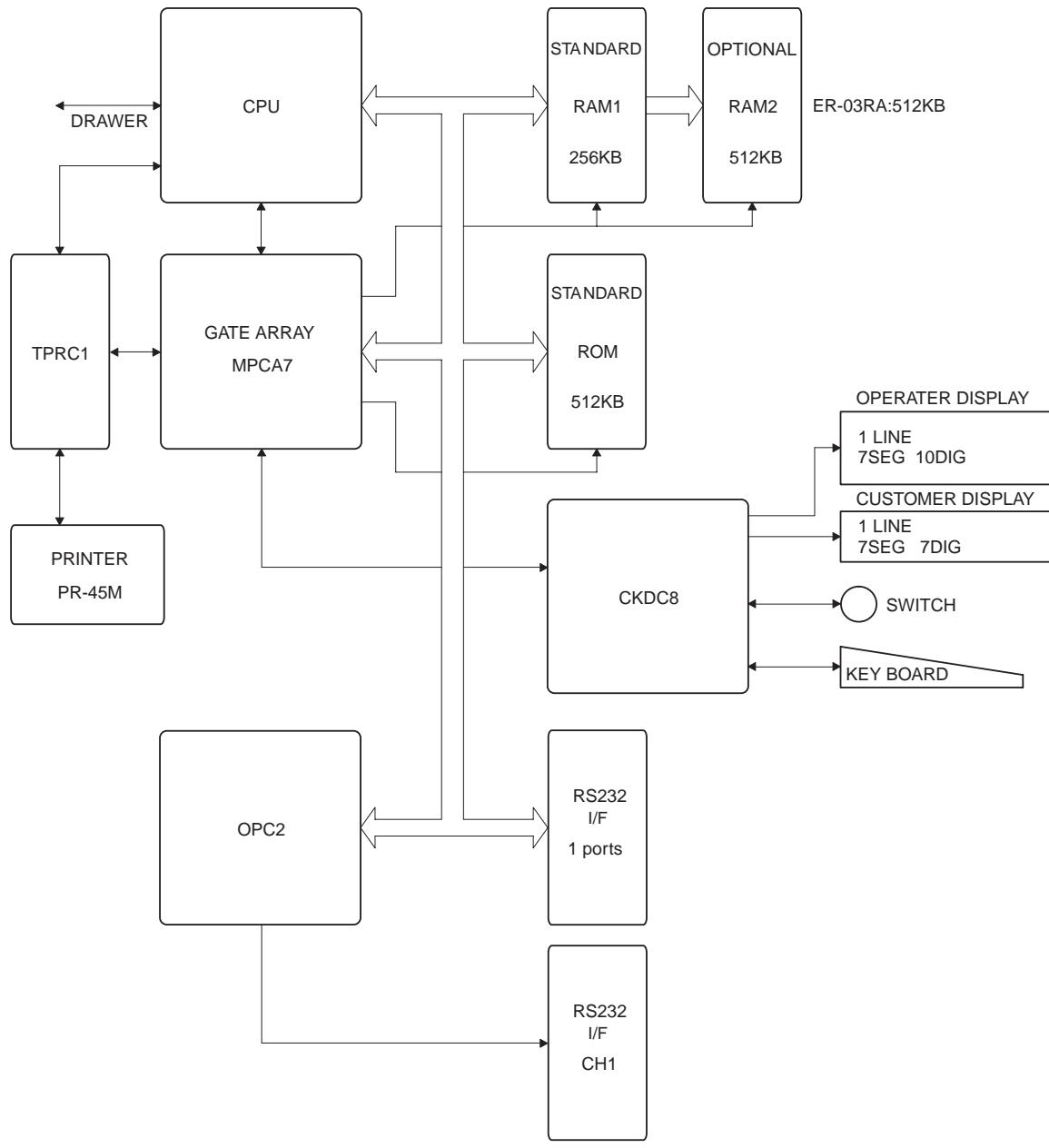
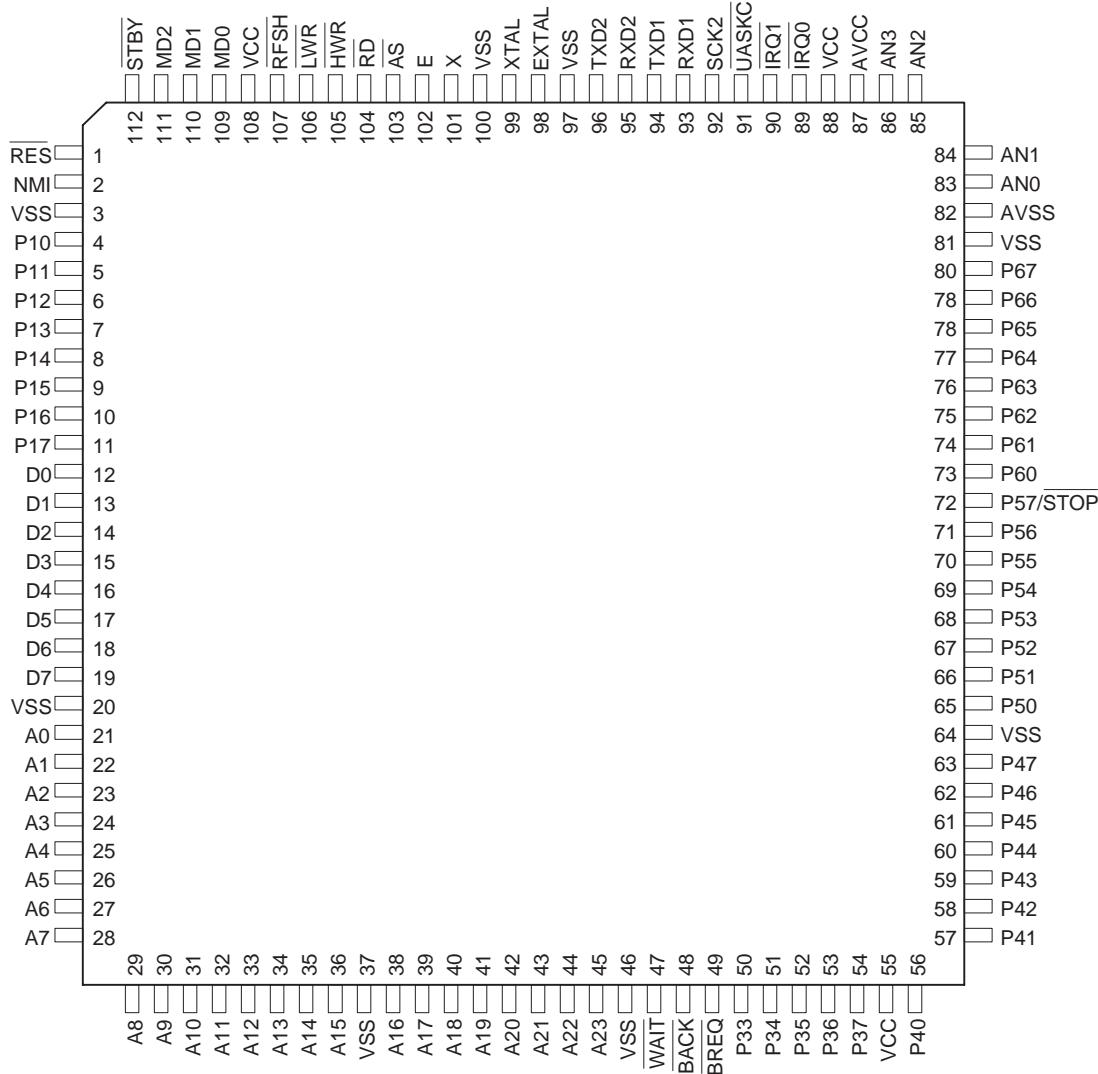


Fig. 1-1

2. Description of main LSI's

2-1. CPU (HD6415108-10)

1) Pin configuration



HD6415108-10 pin configuration

Fig. 2-1

2) Block diagram

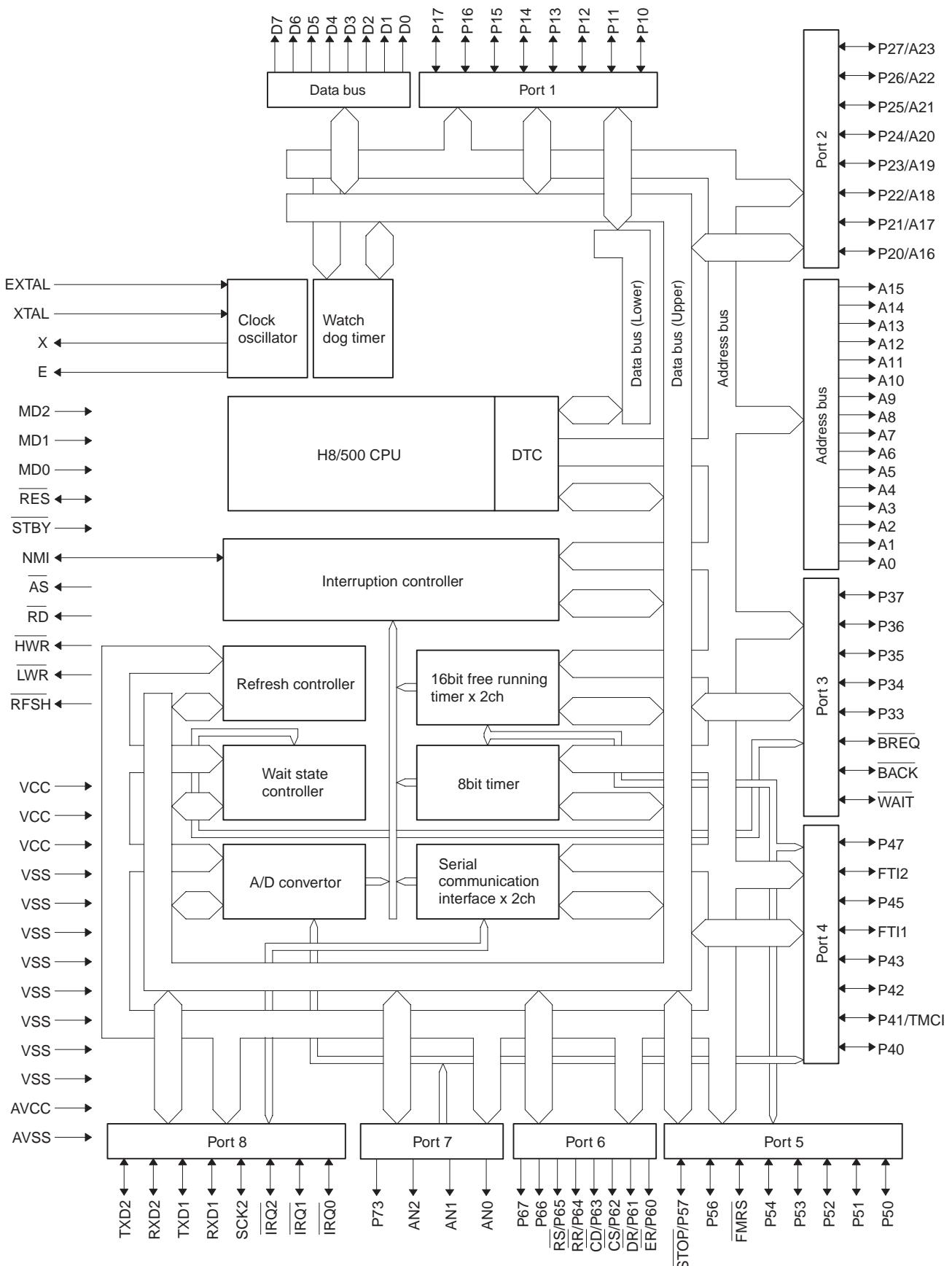


Fig. 2-2

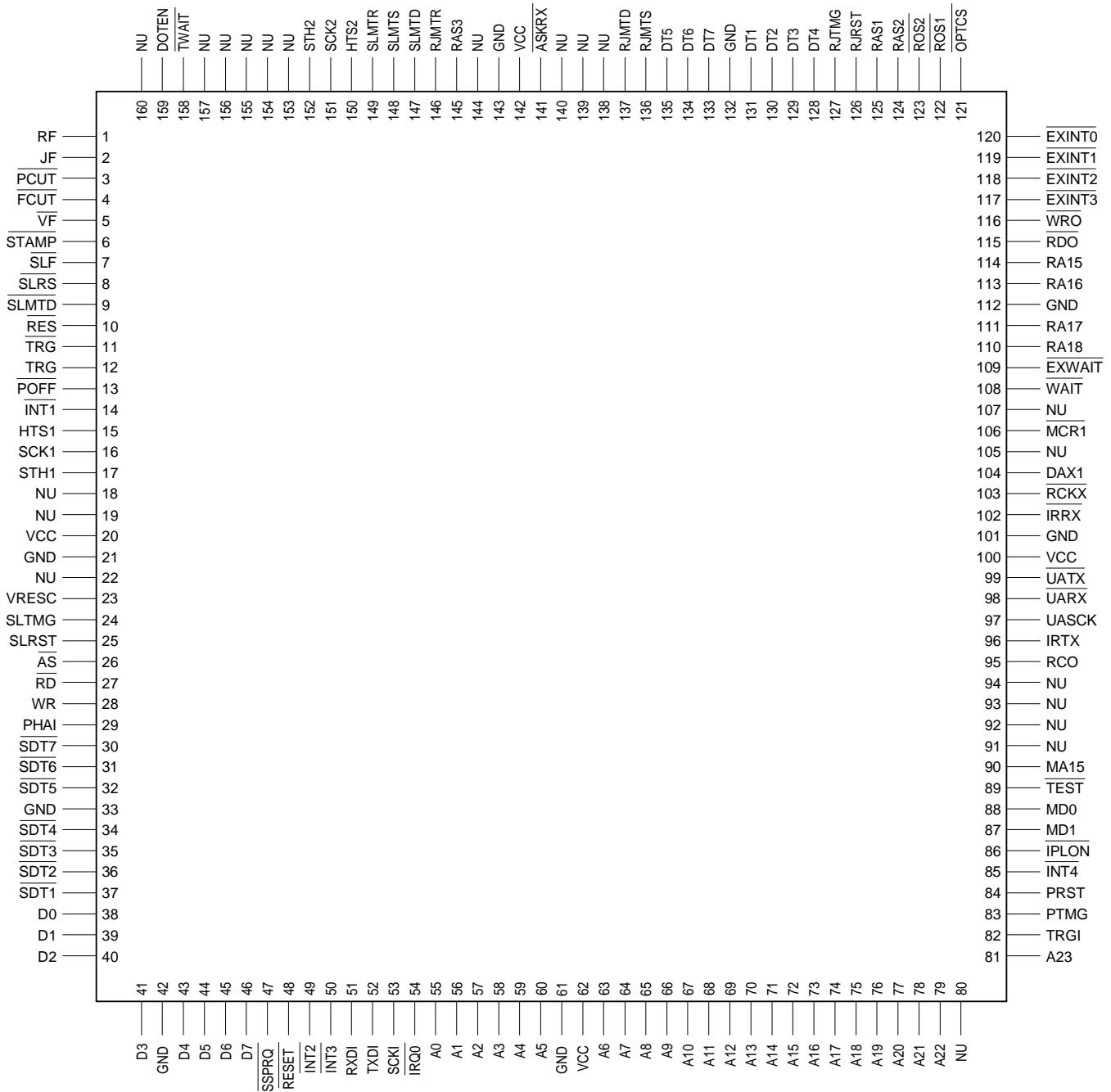
3) Pin description

PIN No.	SYMBOL	SIGNAL NAME	IN/OUT	FUNCTION
1	/RES	/RESET	IN	RESET INPUT from CKDC WUTH BUFFER
2	NMi	NMi	IN	NON-MASKABLE INTERRUPT INPUT FOR SSP INTERRUPT INPUT
3	VSS	VSS		GND
4	P10	ERC	OUT	EVENT READ CANCEL (to CKDC)
5	P11	LDRQ	OUT	LOAD REQUEST (to CKDC)
6	P12	/SHEN	IN	SHIFT ENABLE (from CKDC)
7	P13	/FRES	OUT	FISCAL MEMORY RESET (Nu)
8	P14	BUSY	IN	FISCAL MEMORY BUSY (Nu)
9	P15	/RDY	IN	FISCAL MEMORY READY (Nu)
10	P16	PDS	IN	POP-UP DISPLAY SENSOR (Nu)
11	P17		IN	GND
12	D0	D0	I/O	DATA BUS 0
13	D1	D1	I/O	DATA BUS 1
14	D2	D2	I/O	DATA BUS 2
15	D3	D3	I/O	DATA BUS 3
16	D4	D4	I/O	DATA BUS 4
17	D5	D5	I/O	DATA BUS 5
18	D6	D6	I/O	DATA BUS 6
19	D7	D7	I/O	DATA BUS 7
20	VSS	VSS		GND
21	A0	A0	OUT	ADDRESS BUS 0
22	A1	A1	OUT	ADDRESS BUS 1
23	A2	A2	OUT	ADDRESS BUS 2
24	A3	A3	OUT	ADDRESS BUS 3
25	A4	A4	OUT	ADDRESS BUS 4
26	A5	A5	OUT	ADDRESS BUS 5
27	A6	A6	OUT	ADDRESS BUS 6
28	A7	A7	OUT	ADDRESS BUS 7
29	A8	A8	OUT	ADDRESS BUS 8
30	A9	A9	OUT	ADDRESS BUS 9
31	A10	A10	OUT	ADDRESS BUS 10
32	A11	A11	OUT	ADDRESS BUS 11
33	A12	A12	OUT	ADDRESS BUS 12
34	A13	A13	OUT	ADDRESS BUS 13
35	A14	A14	OUT	ADDRESS BUS 14
36	A15	A15	OUT	ADDRESS BUS 15
37	VSS	VSS		GND
38	A16	A16	OUT	ADDRESS BUS 16
39	A17	A17	OUT	ADDRESS BUS 17
40	A18	A18	OUT	ADDRESS BUS 18
41	A19	A19	OUT	ADDRESS BUS 19
42	A20	A20	OUT	ADDRESS BUS 20
43	A21	A21	OUT	ADDRESS BUS 21
44	A22	A22	OUT	ADDRESS BUS 22
45	A23	A23	OUT	ADDRESS BUS 23
46	VSS	VSS		GND
47	/WAIT	/WAIT	IN	Wait signal from MPCA
48	/BACK	/BACK	OUT	Bus control request acknowl edge
49	/BREQ	/BREQ	IN	Bus control request
50	P33	DOPS	IN	Drawer open sencer signal
51	P34	/DR0	OUT	Drawer open drive signal
52	P35	/DR1	OUT	Option drawer 1 drive signal
53	P36	NU	IN	(Nu) GND
54	P37	NU	IN	(Nu) GND
55	VCC	VCC		+5V
56	P40	/IFV	IN	(Nu) pull-up
57	P41	/PTMG	IN	Printer (PR-45) timing signal from MPCA
58	P42	/TOF	IN	(Nu) pull-up
59	P43	/BOF	IN	(Nu) pull-up

PIN No.	SYMBOL	SIGNAL NAME	IN/OUT	FUNCTION
60	P44	/PRST	IN	Printer (PR-45) Reset signal from MPCA
61	P45	/NEJ	IN	Near END signal jounal
62	P46	NU	IN	(NU) GND
63	P47	/NER	IN	Near END signal receipt
64	VSS	VSS		GND
65	P50	TRG1	OUT	Nu (GND)
66	P51	/PSTOP	OUT	Nu (GND)
67	P52	/CKDCR2	OUT	Nu (GND)
68	P53	OPDS	IN	Nu (GND)
69	P54	FVPON	OUT	Nu (GND)
70	P55	FMRS	IN	Nu (GND)
71	P56	/SLIPLMP	OUT	Nu (GND)
72	P57	/STOP	OUT	Nu (GND)
73	P60	/ERS	OUT	ER signal for RS232 (Equipment Ready)
74	P61	/DRS	IN	DR signal for RS232 (Data set Ready)
75	P62	/CSS	IN	CS signal for RS232 (Clear to Send)
76	P63	/CDS	IN	CD signal for RS232 (Carrier Detect)
77	P64	/RR	OUT	RR signal for RS232 (Ready to Receive) (Nu)
78	P65	/RSS	OUT	RS signal for RS232 (Request to Send)
79	P66	(/RI), /CI	IN	CI signal for RS232 (Calling Indicator)
80	P67	HP	IN	Nu (GND)
81	VSS	VSS		GND
82	AVSS	AVSS	IN	GND
83	AN0	Vrf	IN	Vrf
84	AN1	VHTEST	IN	VH Test input
85	AN2	VPTEST	IN	+24V test input
86	AN3	TM	IN	Thermal head thermistor level test
87	AVCC	AVCC	IN	+5V
88	VCC	VCC		+5V
89	P80	/IRQ0	IN	Interrupt signal 0 from MPCA
90	P81	/IRQ1 (/RSRQ)	IN	Interrupt signal from OPTION PWB
91	P82	/IRQ2	IN	Interrupt signal (Nu) pull-up
92	P83	SCK2	OUT	CKDC & FMC i/F sync shift clock
93	P84	RXD	IN	RS232C RECEIVE DATA
94	P85	TXD	OUT	RS232C SEND DATA
95	P86	RXD2	IN	CKDC, Fiscal memory unit I/F shift input data
96	P87	TXD2	OUT	CKDC, Fiscal memory unit I/F shift output data
97	VSS	VSS		GND
98	EXTAL	EXTAL	IN	X-TAL (19.66MHz)
99	XTAL	XTAL	IN	X-TAL (19.66MHz)
100	VSS	VSS		GND
101	φ	φ	OUT	System clock (9.83MHz)
102	E		OUT	E clock (NU)
103	/AS	/AS	OUT	Address strobe
104	/RD	/RD	OUT	Read
105	/HWR	/WR	OUT	Write
106	/LWR		OUT	Nu
107	/RFSH	/RFSH	OUT	Refresh cycle (NU)
108	VCC	VCC		+5V
109	MD0	MD0	IN	+5V (MODE 3)
110	MD1	MD1	IN	+5V (MODE 3)
111	MD2	MD2	IN	GND (MODE 3)
112	/STBY	/STBY	IN	+5V (Nu)

2-2. G.A (MPCA7)

1) Pin configuration



GATE ARRAY (LZ9AH39)
MPCA7

Fig. 2-3

2) Block diagram

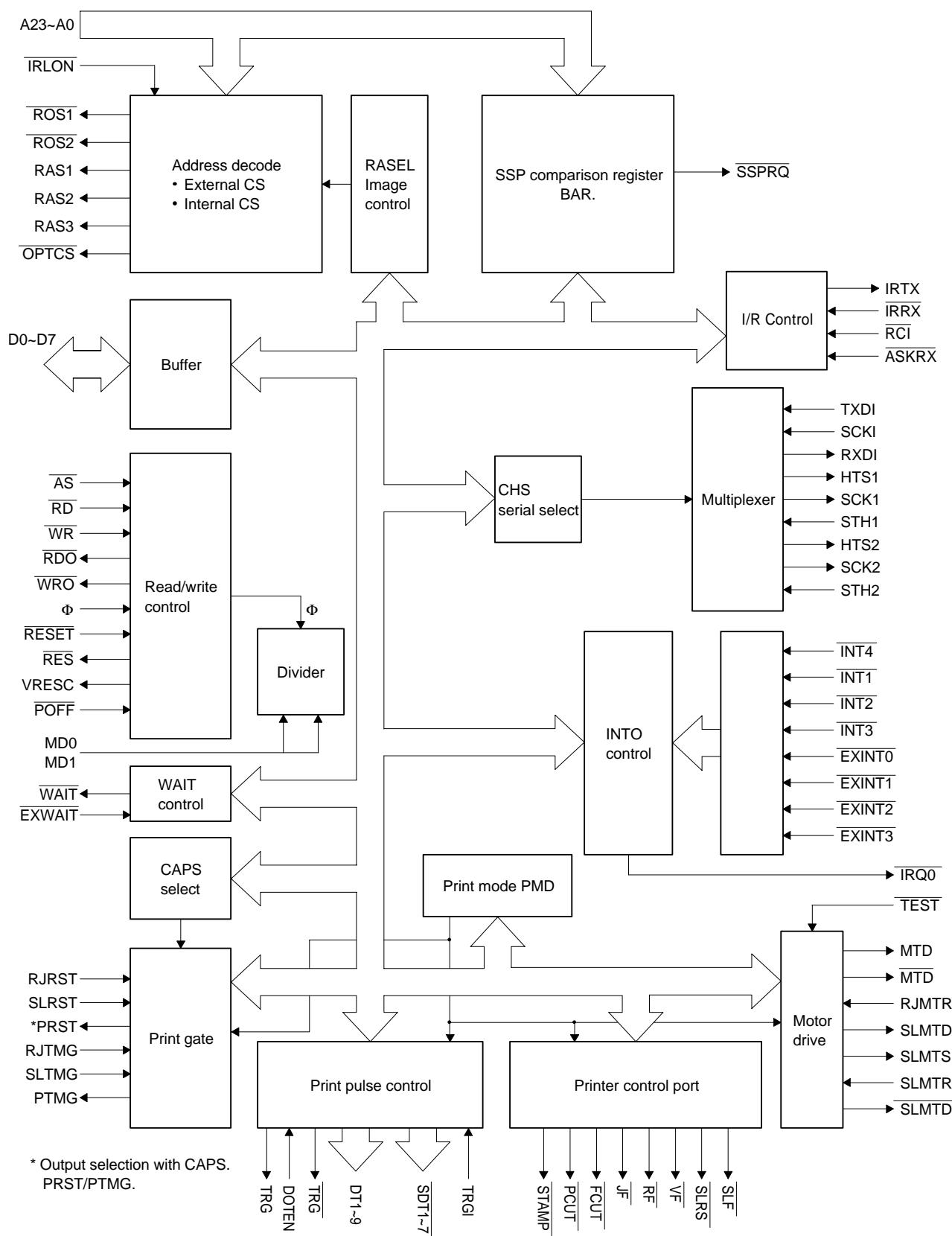


Fig. 2-4

3) Pin description

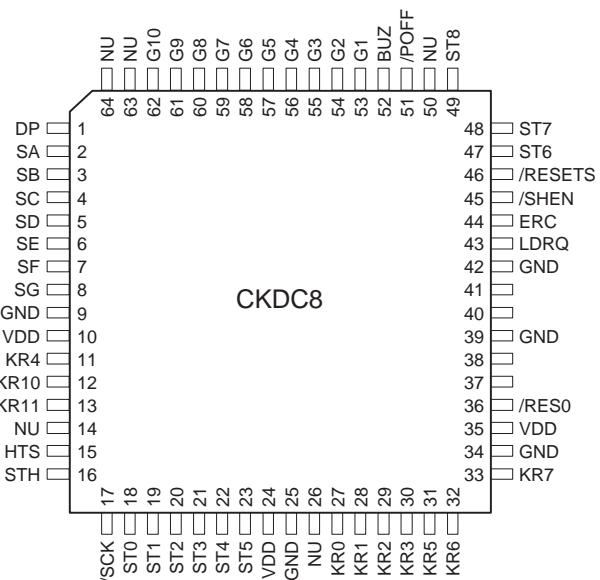
Pin No.	Signal name	In/Out	Function
1	RF	Out	Receipt side paper feed solenoid (NU)
2	JF	Out	Journal side paper feed solenoid (NU)
3	<u>PCUT</u>	Out	Printer partial cut signal (NU)
4	<u>FCUT</u>	Out	Printer auto cut signal (NU)
5	VF	Out	Multi line validation paper feed (NU)
6	STAMP	Out	Printer stamp signal (NU)
7	SLFS	Out	Slip printer paper feed singnal (NU)
8	SLRS	Out	Slip printer release signal (NU)
9	SLMTD	Out	Slip printer motor drive signal (NU)
10	<u>RES</u>	Out	Peripheral output reset
11	<u>TRG</u>	Out	Dot head trigger signal (NU)
12	TRG	Out	Dot head trigger signal (NU)
13	<u>POFF</u>	In	Power off signal input
14	INT1	In	(NU)
15	HTS1	Out	8 bit serial port output (for CKDC8)
16	SCK1	Out	Serial port shift clock output (for CKDC8)
17	STH1	In	8 bit serial port input (for CKDC8)
18	RAS VZ	—	Chip select (NU)
19	—	—	Nu
20	VCC	—	+5V
21	GND	—	GND
22	INTMCR	—	Interrupt (NU)
23	VRESC	Out	Turns active when reset and power down is met
24	SLTMG	In	Slip printer timing signal (NU)
25	SLRST	In	Slip printer reset signal (NU)
26	<u>AS</u>	In	Address strobe
27	<u>RD</u>	In	Read strobe
28	WR	In	Write strobe
29	<u>φ</u>	In	(φ) System clock (9.83 MHz)
30	<u>SDT7</u>	Out	Slip printer printhead drive signal (dot7) (NU)
31	<u>SDT6</u>	Out	Slip printer printhead drive signal (dot6) (NU)
32	<u>SDT5</u>	Out	Slip printer printhead drive signal (dot5) (NU)
33	GND	—	GND
34	<u>SDT4</u>	Out	Slip printer printhead drive signal (dot4) (NU)
35	<u>SDT3</u>	Out	Slip printer printhead drive signal (dot3) (NU)
36	<u>SDT2</u>	Out	Slip printer printhead drive signal (dot2) (NU)
37	<u>SDT1</u>	Out	Slip printer printhead drive signal (dot1) (NU)
38	D0	I/O	Data bus 0
39	D1	I/O	Data bus 1
40	D2	I/O	Data bus 2
41	D3	I/O	Data bus 3
42	GND	—	GND
43	D4	I/O	Data bus 4
44	D5	I/O	Data bus 5
45	D6	I/O	Data bus 6
46	D7	I/O	Data bus 7
47	SPRQ	Out	SSP interrupt request to CPU
48	<u>RESET</u>	In	MPCA reset
49	<u>SHEN</u>	In	Shift enable from CKDC8
50	<u>INT3</u>	In	Interrupt signal (Nu)

Pin No.	Signal name	In/Out	Function
51	RXD2	Out	8 bit serial port output to CPU
52	TXD2	In	8 bit serial port input from CPU
53	SCK2	In	Serial port shift clock input from CPU.
54	<u>IRQ0</u>	Out	Interrupt request to CPU
55	A0	In	Address bus 0
56	A1	In	Address bus 1
57	A2	In	Address bus 2
58	A3	In	Address bus 3
59	A4	In	Address bus 4
60	A5	In	Address bus 5
61	GND	—	GND
62	VCC	—	+5V
63	A6	In	Address bus 6
64	A7	In	Address bus 7
65	A8	In	Address bus 8
66	A9	In	Address bus 9
67	A10	In	Address bus 10
68	A11	In	Address bus 11
69	A12	In	Address bus 12
70	A13	In	Address bus 13
71	A14	In	Address bus 14
72	A15	In	Address bus 15
73	A16	In	Address bus 16
74	A17	In	Address bus 17
75	A18	In	Address bus 18
76	A19	In	Address bus 19
77	A20	In	Address bus 20
78	A21	In	Address bus 21
79	A22	In	Address bus 22
80	<u>LCDC</u>	—	LCD CS (NU)
81	A23	In	Address bus 23
82	TRGI	In	Dot pulse control/drive signal (NU: GND)
83	<u>PTMG</u>	Out	Printer timing signal to CPU
84	<u>PRST</u>	Out	Printer reset signal to CPU
85	<u>RDY</u>	In	Ready from FMC unit
86	<u>IPLON</u>	In	To option connector (NU) +5V
87	MD1	In	Mode select input (GND)
88	MD0	In	Mode select input (GND)
89	<u>TEST</u>	In	+5V
90	MA15	—	Image address 15
91	MA18	—	Nu
92	MA19	—	Nu
93	RCVRDY1	—	Nu: +5V
94	RCVRDY2	—	Nu: +5V
95	RC0	—	Remote control encord signal for CPU (NU)
96	IRTX	—	I/R output for LED (NU)
97	UASCK	—	I/R serial data shift clock (NU)
98	<u>UARX</u>	—	I/R serial data for CPU (NU)
99	<u>UATX</u>	—	I/R serial data from CPU (NU) +5V
100	VCC	—	+5V
101	GND	—	GND
102	<u>IRRX</u>	—	I/R input from I/R unit (NU) +5V
103	<u>RCI</u>	—	I/R input from I/R unit (NU) +5V
104	DAX1	—	System clock (NU)
105	DAX2	—	Nu
106	MCR1	—	Nu

Pin No.	Signal name	In/Out	Function		
107	MCR2	—	Nu		
108	WAIT	Out	Wait request signal		
109	EXWAIT	In	External wait control input signal (NU) +5V		
110	RA18	Out	Nu		
111	RA17	Out	Nu		
112	GND	—	GND		
113	RA16	Out	Nu		
114	RA15	Out	Nu		
115	RDO	Out	Expansion RD signal	Option	
116	WRD	Out	Expansion WR signal		
117	EXINT3	In	RS232C /CD interrupt	Option	
118	EXINT2	In	Option PWB (PULL UP)		
119	EXINT1	In	RS232C /Cl interrupt		
120	EXINT0	In	Option PWB (PULL UP)		
121	OPTCS	Out	Chip select base signal for expansion option	Option	
122	ROS1	Out	ROM 1 chip select signal		
123	ROS2	Out	ROM 2 chip select signal (NU)		
124	RAS2	Out	RAM 2 chip select signal		
125	RAS1	Out	RAM 1 chip select signal		
126	RJRST	In	Printer reset signal		
127	RJTMG	In	FOR TPRC (NU) +5V		
128	DT4	Out	Printer dot signal 4 (NU)		
129	DT3	Out	Printer dot signal 3 (NU)		
130	DT2	Out	Printer dot signal 2 (NU)		
131	DT1	Out	Printer dot signal 1 (NU)	Option	
132	GND	—	GND		
133	DT7	Out	Printer dot signal 7 (NU)		
134	DT6	Out	Printer dot signal 6 (NU)		
135	DT5	Out	Printer dot signal 5 (NU)		
136	MTD	Out	Printer motor drive signal (NU)		
137	MTD	Out	Printer motor drive signal (NU)		
138	DOT9	Out	Printer dot signal 9 (NU)		
139	DOT8	Out	Printer dot signal 8 (NU)		
140	SYNC	—	Nu (+5V)		
141	ASKRX	—	I/R input from I/R unit (NU) Pull-up	Option	
142	VCC	—	+5V		
143	GND	—	GND		
144	—	—	Nu		
145	RAS3	Out	Nu		
146	RJMTR	In	Printer motor lock detection signal (NU) GND		
147	SLMTD	Out	Nu		
148	SLMTS	Out	Nu		
149	SLMTR	In	GND		
150	HTS2	Out	Serial output to FMC unit	Option	
151	SCK2	Out	Serial clock to FMC unit		
152	STH2	In	Serial input to FMC unit		
153	—	—	Nu		
154	—	—	Nu		
155	—	—	Nu		
156	—	—	Nu		
157	—	—	Nu		
158	LCDWT	IN	TPRC wait signal		
159	DOTEN	Out	Dot drive enable signal (Nu)		
160	RASP	—	Nu	Option	

2-3. CKDC8

1) Pin configuration



2) Pin assignment (CKDC8)

PIN NO.	SYMBOL	SIGNAL NAME	IN/OUT	FUNCTION
1	DP	DP	OUT	DISPLAY SEGMENT Dp
2	A	SA	OUT	DISPLAY SEGMENT a
3	B	SB	OUT	DISPLAY SEGMENT b
4	C	SC	OUT	DISPLAY SEGMENT c
5	D	SD	OUT	DISPLAY SEGMENT d
6	E	SE	OUT	DISPLAY SEGMENT e
7	F	SF	OUT	DISPLAY SEGMENT f
8	G	SG	OUT	DISPLAY SEGMENT g
9	VSS0	GND		GND
10	VDD0	VDD		VDD
11	KR4	KR4	IN	KEY RETURN 4
12	KR10	KR10	IN	KEY RETURN (feed clerk MRS sw)
13	KR11	KR11	IN	KEY RETURN (MODE sw)
14	KR8	NU	IN	GND
15	HTS	HTS	IN	
16	STH	STH	OUT	
17	/SCK	/SCK	IN	SHIFT CLOCK
18	ST0	ST0	OUT	KEY STROBE 0
19	ST1	ST1	OUT	KEY STROBE 1
20	ST2	ST2	OUT	KEY STROBE 2
21	ST3	ST3	OUT	KEY STROBE 3
22	ST4	ST4	OUT	KEY STROBE 4
23	ST5	ST5	OUT	KEY STROBE 5
24	VDD1	VDD		VDD
25	AXSS	GND		GND
26	KR9	NU		GND
27	KR0	KR0	IN	KEY RETURN 0
28	KR1	KR1	IN	KEY RETURN 1
29	KR2	KR2	IN	KEY RETURN 2
30	KR3	KR3	IN	KEY RETURN 3
31	KR5	KR5	IN	KEY RETURN 5

PIN NO.	SYMBOL	SIGNAL NAME	IN/OUT	FUNCTION
32	KR6	KR6	IN	KEY RETURN 6
33	KR7	KR7	IN	KEY RETURN 7
34	AVRF	GND		
35	AVDD	VDD		
36	/RESET	/RES0	IN	
37	XT2			
38	XT1			32.768 KHz
39	IC	GND		
40	X2			4.19 MHz
41	X1			
42	VSS1	GND		
43	LDRQ	LDRQ	IN	LORD REQUEST
44	ERC	ERC	IN	EVENT READ CANCEL
45	SHEN	/SHEN	OUT	SHIFT ENABLE
46	/RES1	/RESETS	OUT	SYSTEM TO RESET
47	ST6	ST6	OUT	KEY STROBE 6
48	ST7	ST7	OUT	KEY STROBE 7
49	ST8	ST8	OUT	KEY STROBE 8
50	ST9	NU	OUT	KEY STROBE 9
51	/POFF	/POFF	IN	POWER OFF
52	BUZ	BUZ	OUT	BUZZER
53	T0	G1	OUT	DISPLAY DIGIT 1
54	T1	G2	OUT	DISPLAY DIGIT 2
55	T2	G3	OUT	DISPLAY DIGIT 3
56	T3	G4	OUT	DISPLAY DIGIT 4
57	T4	G5	OUT	DISPLAY DIGIT 5
58	T5	G6	OUT	DISPLAY DIGIT 6
59	T6	G7	OUT	DISPLAY DIGIT 7
60	T7	G8	OUT	DISPLAY DIGIT 8
61	T8	G9	OUT	DISPLAY DIGIT 9
62	T9	G10	OUT	DISPLAY DIGIT 10
63	T10	NU	OUT	DISPLAY DIGIT 11
64	ID	NU	OUT	DISPLAY SEGMENT ▼

2-4. TPRC1 (F258024PC)

1) General

TPRC1 is the LSI circuit of the peripheral circuits of the microcomputer required for thermal printer control.

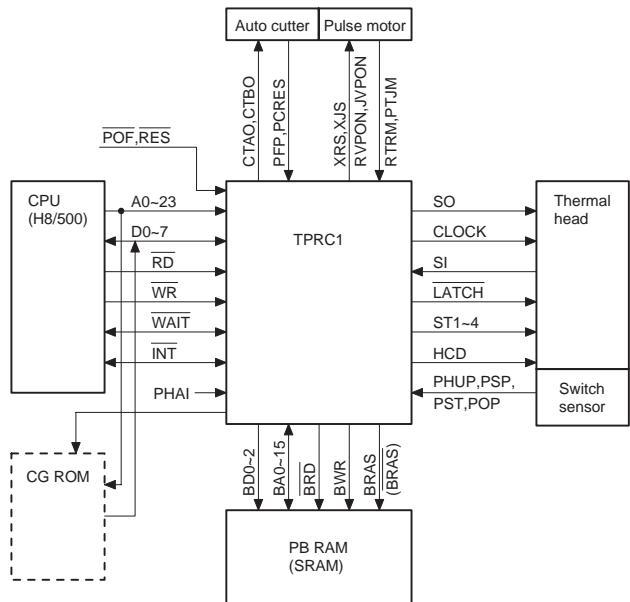


Fig. 2-6

The CPU is designed for use with H8/500. The bus I/F, however, is not restricted to the design concept.

The printer is designed mainly for use with PR-58. However, the thermalhead composition (the dot number and the block number) is rather flexible.

1. Auto cutter (Option)
2. Pulse motor
3. Thermalhead
4. Switch

2) Pin configuration

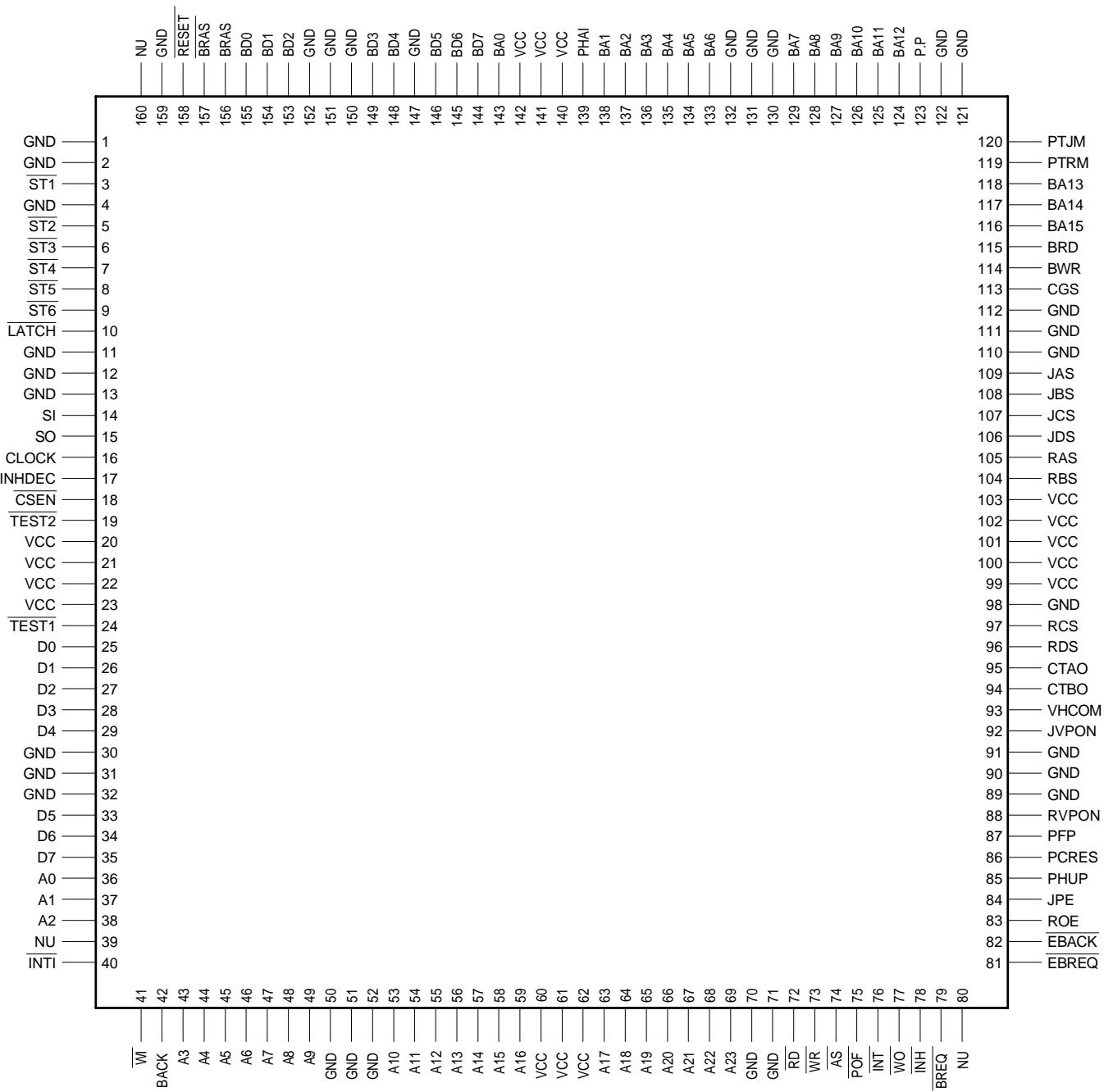
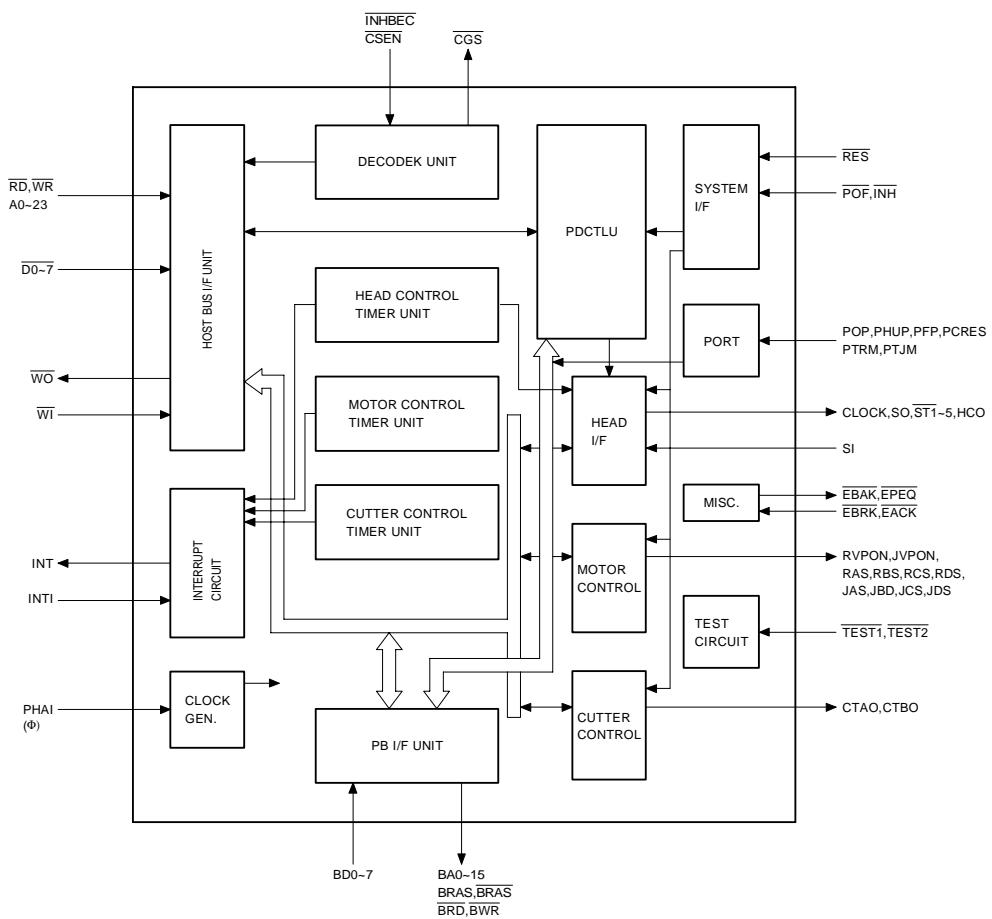


Fig. 2-7

3) Block diagram



TPRC1 BLOCK DIAGRAM

Fig. 2-8

4) Pin description

Pin No.	Signal name	In/Out	Function
1	GND	—	GND
2	GND	—	GND
3	ST1	O	Head drive strobe signal 1
4	GND	—	GND
5	ST2	O	Head drive strobe signal 2
6	ST3	O	Head drive strobe signal 3
7	ST4	O	Head drive strobe signal 4
8	ST5	O	NU
9	ST6	O	NU
10	LATCH	O	Head latch signal
11	GND	—	GND
12	GND	—	GND
13	GND	—	GND
14	SI	I	Data return line, thermalhead -- TPRC1
15	SO	O	Send data from TPRC1 to thermalhead Data from PB-RAM or zero data are outputted at the falling of CLOCK signal. 16
16	CLOCK	O	Thermalhead CLOCK signal SO is outputted at the edge of I → O, and is taken at the edge of o → I.
17	INHDEC	I	GND

Pin No.	Signal name	In/Out	Function
18	CSEN	I	GND
19	TEST2	I	+5V internal counter timer test pin
20	Vcc	—	+5V
21	Vcc	—	+5V
22	Vcc	—	+5V
23	Vcc	—	+5V
24	TEST1	I	+5V internal counter timer test pin
25	D0	I/O	Data bus 0: Internal register, print buffer data IO
26	D1	I/O	Data bus 1: Internal register, print buffer data IO
27	D2	I/O	Data bus 2: Internal register, print buffer data IO
28	D3	I/O	Data bus 3: Internal register, print buffer data IO
29	D4	I/O	Data bus 4: Internal register, print buffer data IO
30	GND	—	GND
31	GND	—	GND
32	GND	—	GND
33	D5	I/O	Data bus 5: Internal register, print buffer data IO

Pin No.	Signal name	In/Out	Function
34	D6	I/O	Data bus 6: Internal register, print buffer data IO
35	D7	I/O	Data bus 7: Internal register, print buffer data IO
36	A0	I	Address bus 0
37	A1	I	Address bus 1
38	A2	I	Address bus 2
39	TPRCRQ2	—	Request signal
40	INTI	I	+5V
41	WI	I	+5V
42	BACK	I	BACK
43	A3	I	Address bus 3
44	A4	I	Address bus 4
45	A5	I	Address bus 5
46	A6	I	Address bus 6
47	A7	I	Address bus 7
48	A8	I	Address bus 8
49	A9	I	Address bus 9
50	GND	—	GND
51	GND	—	GND
52	GND	—	GND
53	A10	I	Address bus 10
54	A11	I	Address bus 11
55	A12	I	Address bus 12
56	A13	I	Address bus 13
57	A14	I	Address bus 14
58	A15	I	Address bus 15
59	A16	I	Address bus 16
60	Vcc	—	+5V
61	Vcc	—	+5V
62	Vcc	—	+5V
63	A17	I	Address bus 17
64	A18	I	Address bus 18
65	A19	I	Address bus 19
66	A20	I	Address bus 20
67	A21	I	Address bus 21
68	A22	I	Address bus 22
69	A23	I	Address bus 23
70	GND	—	GND
71	GND	—	GND
72	RD	I	Read strobe signal: Gate enable of data bus D0 - D7 tri-state buffer
73	WR	I	Write strobe signal: Write enable into the internal register and the print buffer.
74	AS	I	AS
75	POF	I	Power off signal
76	INT	O	Interrupt signal
77	WO	O	Wait request signal to the CPU
78	INH	I	Head drive inhibit
79	BREQ	O	Bus request to CPU
80	—	—	NU
81	EBREQ	I	Bus request from option
82	E BACK	O	Bus acknowledge to option
83	RPE	I	Receipt paper empty

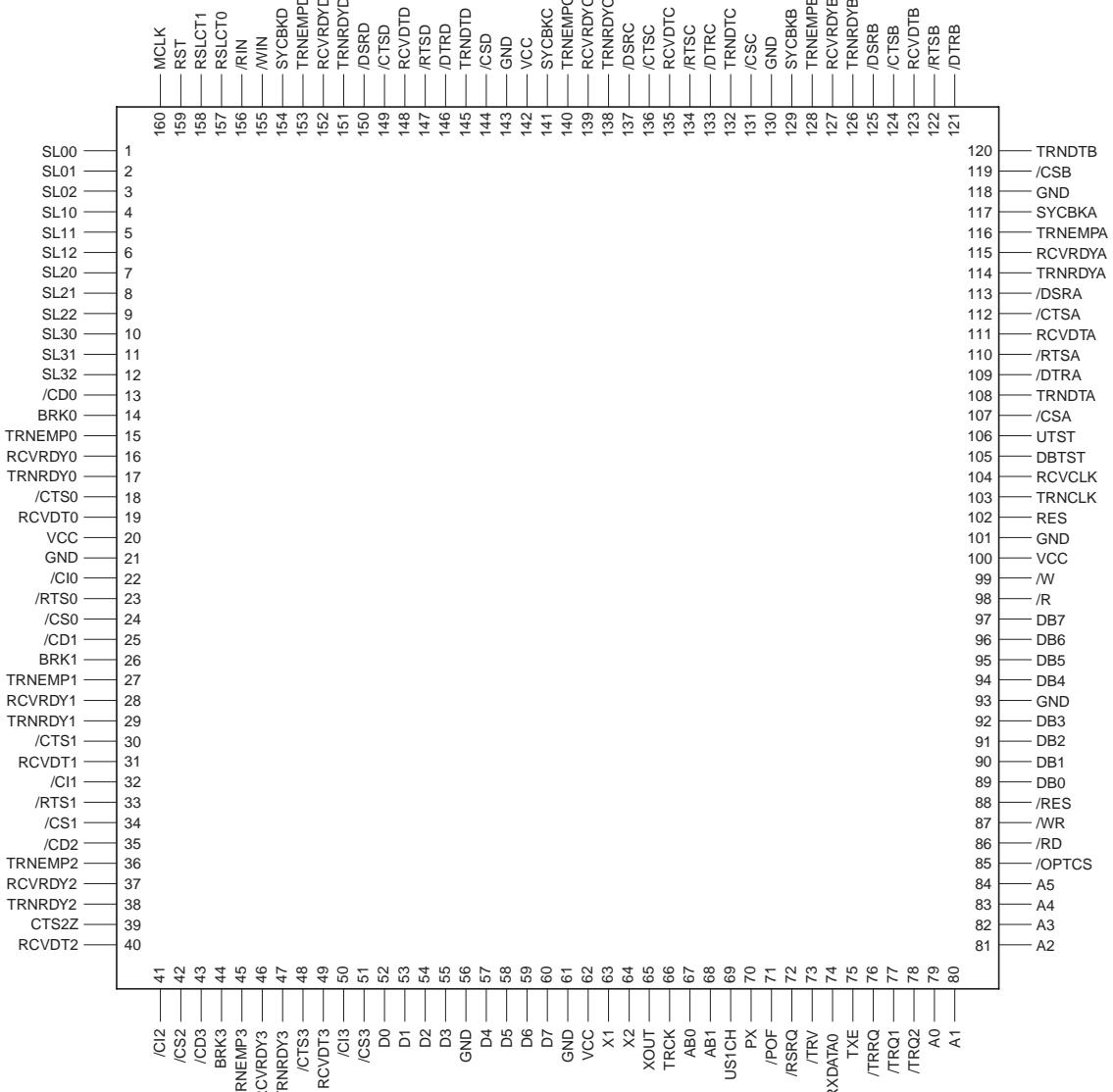
Pin No.	Signal name	In/Out	Function
84	JPE	I	Journal paper empty
85	PHUP	I	Printer head up
86	PCRES	I	Auto cutter unit reset signal input (Nu)
87	PFP	I	Auto cutter unit FP signal input (Nu)
88	RPON	O	Receipt side paper feed pulse motor common power control signal (Nu)
89	GND	—	GND
90	GND	—	GND
91	GND	—	GND
92	JVPON	O	Journal side paper feed pulse motor common power control signal (Nu)
93	VHCOM	O	Head drive common power control
94	CTBO	O	Cutter motor control signal (Nu)
95	CTAO	O	Cutter motor control signal (Nu)
96	RDS	O	Receipt side paper feed pulse motor drive signal, phase D
97	RCS	O	Receipt side paper feed pulse motor drive signal, phase C
98	GND	—	+5V
99	Vcc	—	+5V
100	Vcc	—	+5V
101	Vcc	—	+5V
102	Vcc	—	+5V
103	Vcc	—	+5V
104	RBS	O	Receipt side paper feed pulse motor drive signal, phase B
105	RAS	O	Receipt side paper feed pulse motor drive signal, phase A
106	JDS	O	Journal side paper feed pulse motor drive signal, phase D
107	JCS	O	Journal side paper feed pulse motor drive signal, phase C
108	JBS	O	Journal side paper feed pulse motor drive signal, phase B
109	JAS	O	Journal side paper feed pulse motor drive signal, phase A
110	GND	—	GND
111	GND	—	GND
112	GND	—	GND
113	CGS	O	NU
114	BWR	O	PB-RAM write strobe signal
115	BRD	O	PB-RAM read strobe signal
116	BA15	O	NU
117	BA14	O	Address 14 for PB-RAM
118	BA13	O	Address 13 for PB-RAM
119	PTRM	I	Receipt motor connector sens signal
120	PTJM	I	Journal motor connector sens signal
121	GND	—	GND
122	GND	—	GND
123	POPI	O	GND
124	BA12	O	Address bus 12 for PB-RAM
125	BA11	O	Address bus 11 for PB-RAM
126	BA10	O	Address bus 10 for PB-RAM
127	BA9	O	Address bus 9 for PB-RAM
128	BA8	O	Address bus 8 for PB-RAM
129	BA7	O	Address bus 7 for PB-RAM

Pin No.	Signal name	In/Out	Function
130	GND	—	GND
131	GND	—	GND
132	GND	—	GND
133	BA6	O	Address bus 6 for PB-RAM
134	BA5	O	Address bus 5 for PB-RAM
135	BA4	O	Address bus 4 for PB-RAM
136	BA3	O	Address bus 3 for PB-RAM
137	BA2	O	Address bus 2 for PB-RAM
138	BA1	O	Address bus 1 for PB-RAM
139	PHAI	I	TPRC1 clock input pin (9.83 MHz)
140	Vcc	—	+5V
141	Vcc	—	+5V
142	Vcc	—	+5V
143	BA0	O	Address bus 0 for PB-RAM

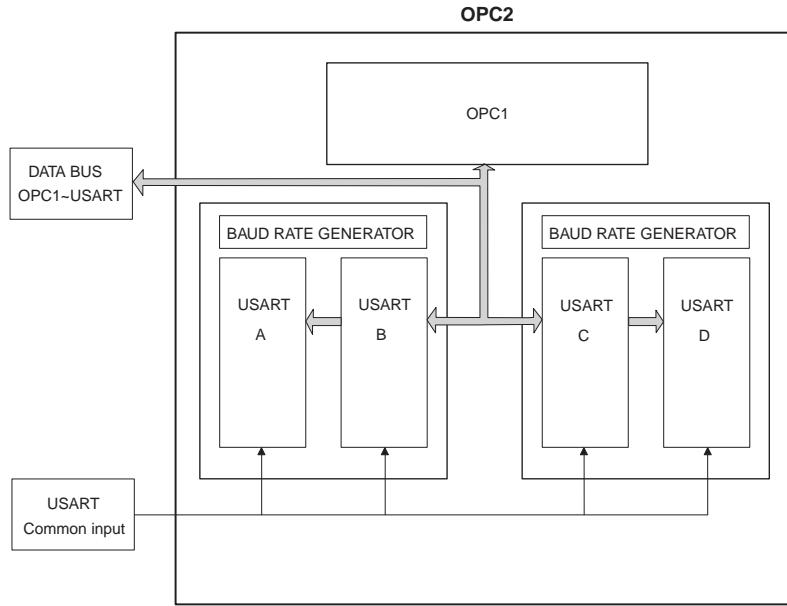
Pin No.	Signal name	In/Out	Function
144	BD7	I/O	Data bus 7 for PB-RAM
145	BD6	I/O	Data bus 6 for PB-RAM
146	BD5	I/O	Data bus 5 for PB-RAM
147	GND	—	GND
148	BD4	I/O	Data bus 4 for PB-RAM
149	BD3	I/O	Data bus 3 for PB-RAM
150	GND	—	GND
151	GND	—	GND
152	GND	—	GND
153	BD2	I/O	Data bus 2 for PB-RAM
154	BD1	I/O	Data bus 1 for PB-RAM
155	BD0	I/O	Data bus 0 for PB-RAM
156	BRAS	O	PB-RAM chip select: Active HIGH (Nu)
157	BRAS	O	PB-RAM chip select: Active LOW
158	RESET	I	TPRC1 reset signal
159	GND	—	GND
160	NU	—	GND

2-5. OPC2

1) Pin configuration



2) Block diagram



3) Pin description

Pin NO.	Name	ER-A770	I/O	Description
1	SL00	VCC	ISU	RS-232/UNIT0 channel select
2	SL01	GND	ISU	
3	SL02	GND	ISU	
4	SL10	GND	ISU	
5	SL11	GND	ISU	RS-232/UNIT1 channel select
6	SL12	GND	ISU	
7	SL20	GND	ISU	
8	SL21	GND	ISU	
9	SL22	GND	ISU	RS-232/UNIT2 channel select
10	SL30	GND	ISU	
11	SL31	GND	ISU	
12	SL32	GND	ISU	
13	/CD0	/DCD1	IS	RS-232 control signal /CD input
14	BRK0	BRK1	IS	RS-232 break signal
15	TRNEMPO	TRENMP1	IS	RS-232 transmission buffer empty signal
16	RCVRDY0	RCVRDY1	IS	RS-232 data reception enable signal
17	TRNRDY0	TRNRDY1	IS	RS-232 transmission enable signal
18	/CTS0	/CTS1	IS	RS-232 clear to send signal
19	RCVDT0	RCVDT1	IS	RS-232 reception data signal
20	VCC	VCC		+5V
21	GND	GND		GND
22	/CI0	/CI1	IS	RS-232 control signal /CI input
23	/RTS0	/RTS1	O	RS-232 request to send signal
24	/CS0	/CS1	O	RS-232 chip select signal
25	/CD1	/DCD2	IS	RS-232 control signal /CD input

Pin NO.	Name	ER-A770	I/O	Description
26	BRK1	BRK2	IS	GND
27	TRNEMP1	TRENMP2	IS	GND
28	RCVRDY1	RCVRDY2	IS	GND
29	TRNRDY1	TRNRDY2	IS	GND
30	/CTS1	/CTS2	IS	+5V
31	RCVDT1	RCVDT2	IS	RS-232 reception data signal
32	/CI1	/CI2	IS	RS-232 control signal /CI input
33	/RTS1	/RTS2	O	RS-232 request to send signal
34	/CS1	/CS2	O	RS-232 chip select signal
35	/CD2	VCC	IS	+5V
36	TRNEMP2	TRENMP3	IS	GND
37	RCVRDY2	RCVRDY3	IS	GND
38	TRNRDY2	TRNRDY3	IS	GND
39	CTS2Z	/CTS3	IS	+5V
40	RCVDT2	RCVDT3	IS	GND
41	/CI2	VCC	IS	+5V
42	/CS2	/CS3	O	NU
43	/CD3	/SINT	IS	RS-232: /CD, IN-LINE : /P1
44	BRK3	GND	IS	GND
45	TRNEMP3	GND	IS	GND
46	RCVRDY3	GND	IS	GND
47	TRNRDY3	GND	IS	GND
48	/CTS3	GND	IS	GND
49	RCVDT3	GND	IS	GND
50	/CI3	GND	IS	GND
51	/CS3	/SRCS	O	RS-232/INLINE chip select signal
52	D0	D0	IO	Data bus (CPU)
53	D1	D1	IO	Data bus (CPU)

Pin NO.	Name	ER-A770	I/O	Description
54	D2	D2	IO	Data bus (CPU)
55	D3	D3	IO	Data bus (CPU)
56	GND	GND		GND
57	D4	D4	IO	Data bus (CPU)
58	D5	D5	IO	Data bus (CPU)
59	D6	D6	IO	Data bus (CPU)
60	D7	D7	IO	Data bus (CPU)
61	GND	GND		GND
62	VCC	VCC		+5V
63	X1	NC	O OS14	NC
64	X2	#	I OS14	System clock
65	XOUT	CLK_USART	O	Clock (USART)
66	TRCK	NC	O	NC
67	AB0	AH0	O	Address bus for USART
68	AB1	AH1	O	Address bus for USART
69	US1CH	GND	IS	GND
70	PX	NC	O	NC
71	/POF	/POFF	IS	POFF signal
72	/RSRQ	/IRQ1	3S	RS232 INTRRUPT
73	/TRV	GND	IS	GND
74	RXDATA0	NC	O	NC
75	TXE	/SRESET	O	INLINE SOFT RESET
76	/TRRQ	/TRQ2	3S	INLINE INTRRUPT
77	/TRQ1	/TRQ1	ON6	TIMER INTRRUPT (RS232)
78	/TRQ2	NC	ON6	TIMER INTRRUPT (INLINE)
79	A0	A0	I	Address bus for CPU
80	A1	A1	I	Address bus for CPU
81	A2	A2	I	Address bus for CPU
82	A3	A3	I	Address bus for CPU
83	A4	A4	I	Address bus for CPU
84	A5	A5	I	Address bus for CPU
85	/OPTCS	/OPTCS	I	Option chip select (from MPCA)
86	/RD	/RDO	I	Read signal (from CPU)
87	/WR	/WRO	I	Write signal (from CPU)
88	/RES	/RES	IS	Reset signal (from CPU)
89	DB0	DB0	IO	DATA BUS (USART)
90	DB1	DB1	IO	DATA BUS (USART)
91	DB2	DB2	IO	DATA BUS (USART)
92	DB3	DB3	IO	DATA BUS (USART)
93	GND	GND		GND
94	DB4	DB4	IO	DATA BUS (USART)
95	DB5	DB5	IO	DATA BUS (USART)
96	DB6	DB6	IO	DATA BUS (USART)
97	DB7	DB7	IO	DATA BUS (USART)
98	/R	/RDH	O	Read signal (to USART)

Pin NO.	Name	ER-A770	I/O	Description
99	/W	/WRH	O	Write signal (to USART)
100	VCC	VCC		+5V
101	GND	GND		GND
102	RES	RES USART	O	Reset signal (to USART)
103	TRNCLK	GND	I	GND
104	RCVCLK	GND	I	GND
105	DBTST	/SRCS	ID	RS-232/INLINE USART chip select
106	UTST	VCC	ID	+5V
107	/CSA	/CS1	IS	USART_A chip select
108	TRNDTA	TXD1	O	RS-232 transmission data signal
109	/DTRA	/DTR1	O	RS-232 data terminal ready signal
110	/RTSA	NC	O	NC
111	RCVDTA	RCVDT1	IS	RS-232 reception data signal
112	/CTSA	GND	IS	GND
113	/DSRA	/DSR1	IS	RS-232 data set ready signal
114	TRNRDYA	TRNRDY1	O	RS-232 data transmission enable signal
115	RCVRDYA	RCVRDY1	O	RS-232 data reception enable signal
116	TRNEMPA	TRNEMP1	O	RS-232 transmission buffer empty signal
117	SYCBKA	BRK1	IO	Break code detection signal
118	GND	GND		GND
119	/CSB	/CS2	IS	USART_B chip select
120	TRNDTB	TXD2	O	NC
121	/DTRB	/DTR2	O	NC
122	/RTSB	NC	O	NC
123	RCVDTB	RCVDT2	IS	GND
124	/CTSB	GND	IS	GND
125	/DSRB	/DSR2	IS	GND
126	TRNRDYB	TRNRDY2	O	NC
127	RCVRDYB	RCVRDY2	O	NC
128	TRNEMPB	TRNEMP2	O	NC
129	SYCBKB	BRK2	IO	NC
130	GND	GND		GND
131	/CSC	/CS3	IS	USART_C chip select
132	TRNDTC	TXD3	O	NC
133	/DTRC	/DTR3	O	NC
134	/RTSC	/RTS3	O	NC
135	RCVDTc	RCVDT3	IS	GND
136	/CTSC	GND	IS	GND
137	/DSRC	/DSR3	IS	GND
138	TRNRDYC	TRNRDY3	O	NC
139	RCVRDYC	RCVRDY3	O	NC
140	TRNEMPC	TRNEMP3	O	NC
141	SYCBKC	NC	IO	NC

Pin NO.	Name	ER-A770	I/O	Description
142	VCC	VCC		+5V
143	GND	GND		GND
144	/CSD	VCC	IS	+5V
145	TRNDTD	NC	O	NC
146	/DTRD	NC	O	NC
147	/RTSD	NC	O	NC
148	RCVDTD	GND	IS	GND
149	/CTSD	GND	IS	GND
150	/DSRD	GND	IS	GND
151	TRNRDYD	NC	O	NC
152	RCVRDYD	NC	O	NC
153	TRNEMPD	NC	O	NC
154	SYCBKD	NC	IO	NC
155	/WIN	/WRH	I	Write signal
156	/RIN	/RDH	I	Read signal
157	RSLCT0	AH0	I	Address bus
158	RSLCT1	AH1	I	Address bus
159	RST	RES USART	IS	Reset signal
160	MCLK	CLK USART	I	Clock (4.91MHz)

- I TTL input
- ID TTL input with pull down
- IS TTL Schmidt input
- ISU TTL Schmidt input with pull up
- IO TTL I/O
- 3S 3-state Buffer (6mA)
- ON6 Open drain (6mA)

3. Clock generator

1) CPU (HD64151010FX)

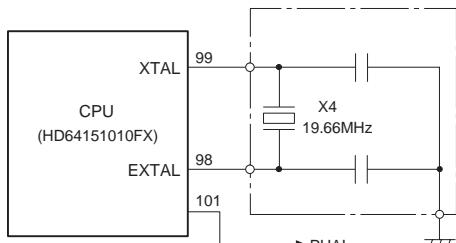


Fig. 3-1

Basic clock is supplied from a 19.66 MHz ceramic oscillator. The CPU contains an oscillation circuit from which the basic clock is internally driven. If the CPU was not operating properly, the signal does not appear on this line in most cases.

2) CKDC8 oscillation circuit

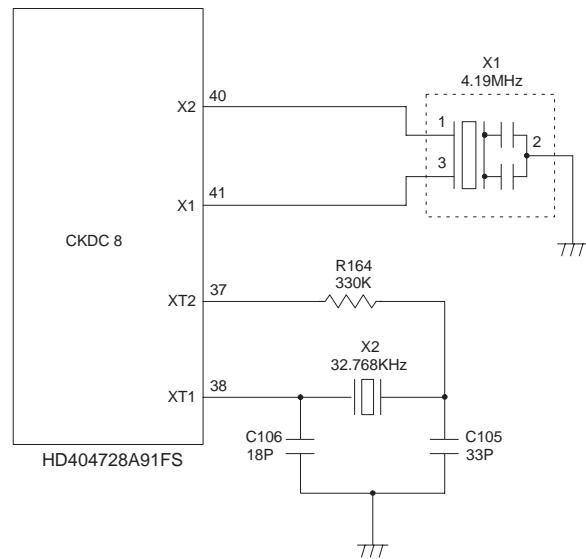


Fig. 3-2

Two oscillators are connected to the CKDC8.

The main clock X1 generates 4.19MHz which is used during power on.

When power is turned off, the CKDC8 goes into the standby mode and the main clock stops.

The sub-clock X2 generates 32.768KHz which is primarily used to update the internal RTC (real time clock). During the standby mode, it keeps oscillating to update the clock and monitoring the power recovery.

4. Reset (POFF) circuit

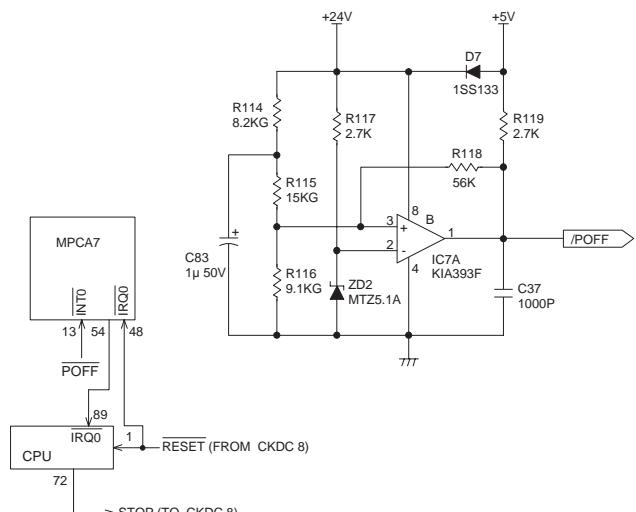
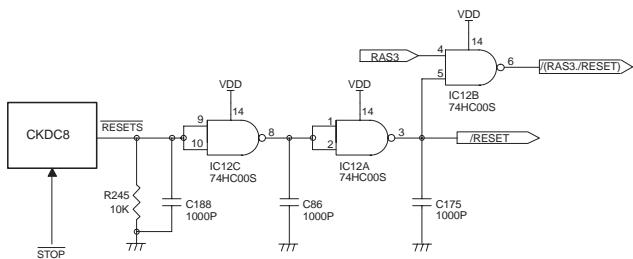


Fig. 4-1

In order to prevent memory loss at a time of power off and power supply failure of the ECR, the power supply condition is monitored at all times. When a power failure is met, the CPU suspends the execution of the current program and immediately executes the power-off program to save the data in the CPU registers in the external S-RAM with the signal STOP forced low to prepare for the power-off situation. The signal STOP is supplied to the CKDC8 as signal RESET to reset the devices.

This circuit monitors +24V supply voltage.

The voltage at the (-) pin of the comparator IC7A is always maintained to 5.1V by means of the zener diode ZD2, while +24V supply voltage is divided through the resistors R114, R115 and R116, and is applied to the (+) pin. When normal +24V is in supply, 6.8V is supplied to the (+) pin, therefore, signal \overline{POFF} is at a high level. When +24V supply voltage decreases due to a power off or any other reason, the voltage at the (+) pin also decreases. When +24V supply voltage drops, the voltage at the (+) pin drops below +5.1V, which causes \overline{POFF} to go low, thus predicting the power-off situation.



The STOP signal from the CPU is converted into the RESETS signal by the CKDC8.

The RESETS signal from the CKDC8 is converted into the /RESET signal at the gate backed-up by the VRAM power, performing the system reset.

5. Memory control

1) Memory map

① All range memory map

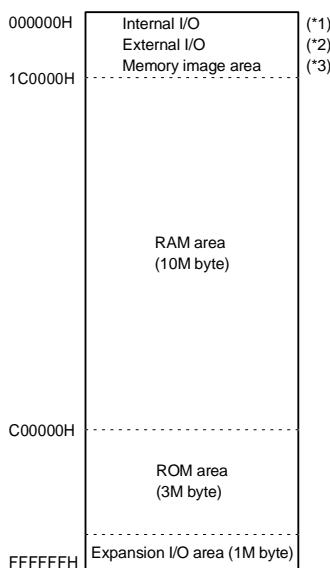


Fig. 5-1

- (*1) "Internal I/O" means the registers in the H8/510.
- (*2) "External I/O" means the base system I/O area to be addressed in page 0.
- (*3) "Memory image area" means the lower 32KB of ROM area which is projected to 000000H ~ 007FFFFH for allowing reset start and other vector addressing, or the lower 32KB of ROM area which is projected to 008000H ~ 00FE7FH for allowing 0 page addressing of work RAM area.
- (*4) "Expansion I/O" means expansion I/O device area which is addressed to area other than page 0.

② 0 page memory map

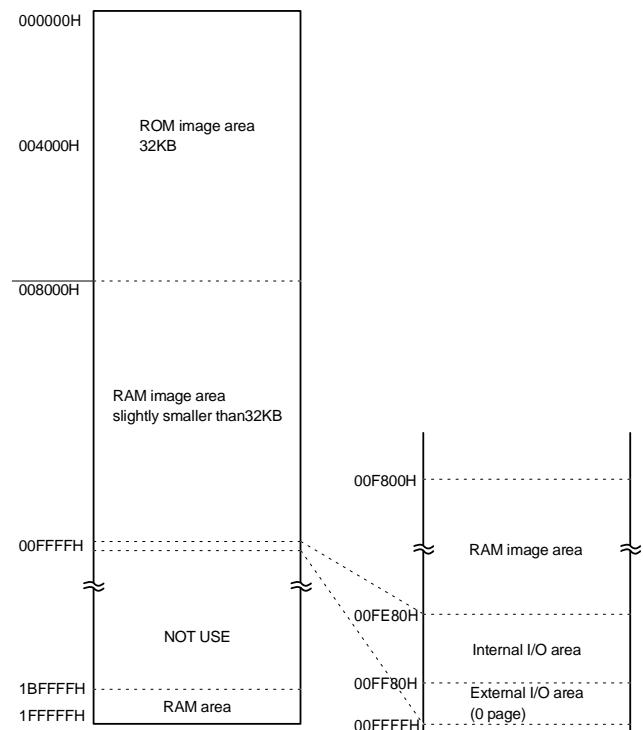


Fig. 5-2

- ROM image area: Image is formed in ROM area address C00000H to C07FFFH. This area is identical to IPL ROM area which will be separately developed.

- RAM image area: Image is formed in RAM area address 1F0000H to 1F7E7FH. (*Note)

* Note: Image can be formed in lower 32KB of RAS2.

③ ROM area memory map

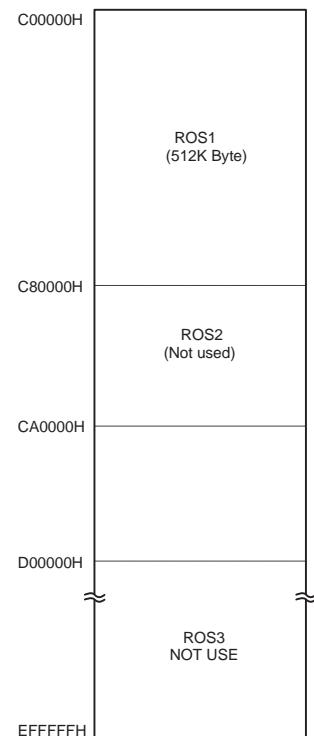


Fig. 5-3

④ RAM area memory map

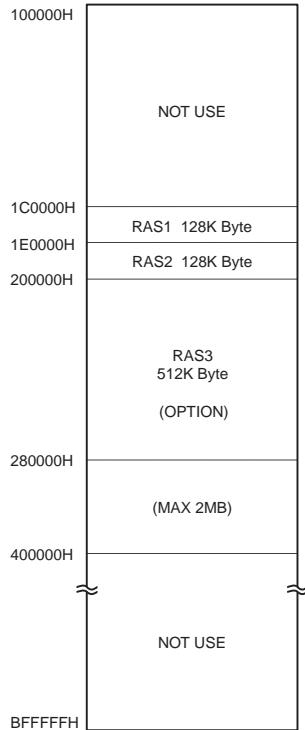


Fig. 5-4

* Note: RAS2 signal is formed as OR in the image area of 0 page.
(lower32KB).

⑤ I/O area memory map

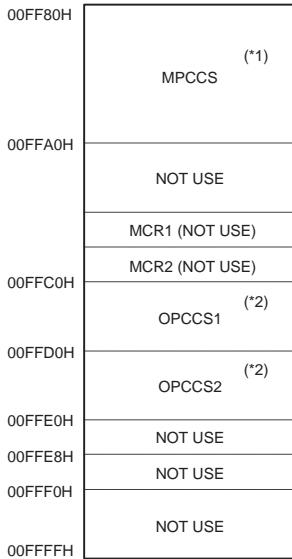


Fig. 5-5

- * Note 1: MPCCS signal is the base signal for MPCA7 internal registerdecoding, and does not exist as an internal signal.
- * Note 2: OPCCS1 and OPCCS2 signals are decoded in the OPC (optionperipheral controller) using the base signal OPTCS for optiondecoding. They does not exist as external signals.

2) Block diagram

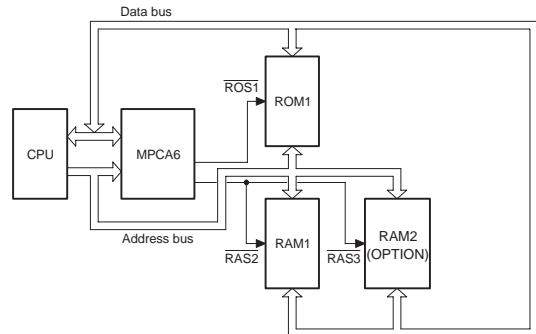


Fig. 5-6

① ROM control

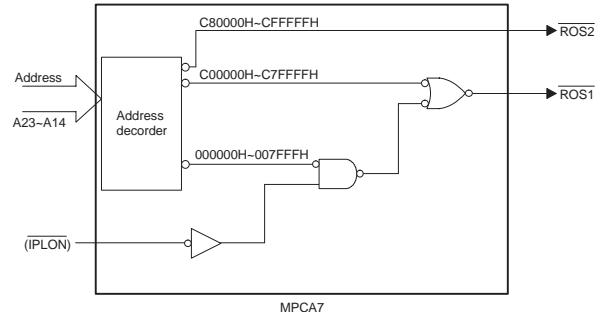


Fig. 5-7

IPLON: IPL board detection signal incorporated in the option slot.
Note used in the ER-A445P. (Not used)

Access is performed with two ROM chip select signals ROS1 and ROS2, which decode 512KB address area respectively to access max. 4MB ROM.

② RAM control

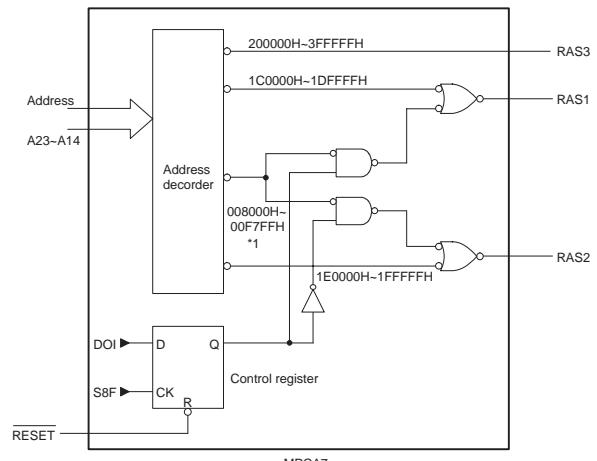


Fig. 5-8

Access is performed with two RAM chip select signals, RAS2 and RAS3. The control register in MPCA7 allows selection of pageimage memory area. (RAS1 is selected for initializing.)

* : For 0 page image area, selection between RAS2 and RAS3 can be made with the control register. The 0 page control register performs initializing at the timing of no stack process immediately after resetting.

6. SSP circuit

1) Block diagram

This is the circuit employed to do the Special Service Preset(SSP).

(Block diagram)

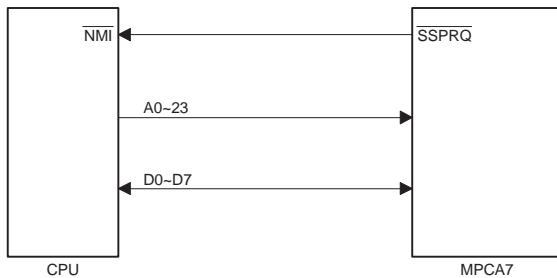


Fig. 6-1

(MPCA7 block diagram)

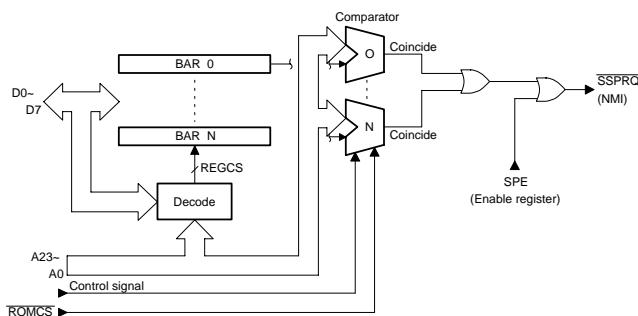


Fig. 6-2

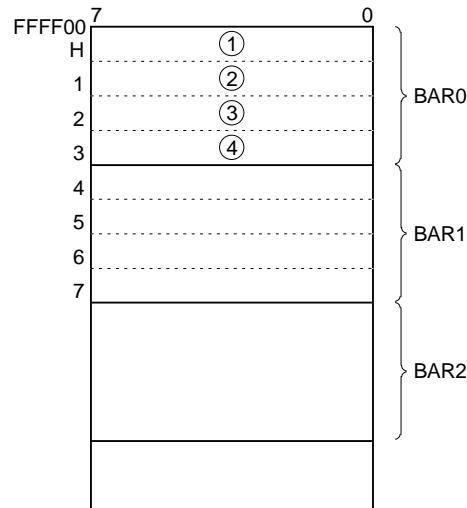
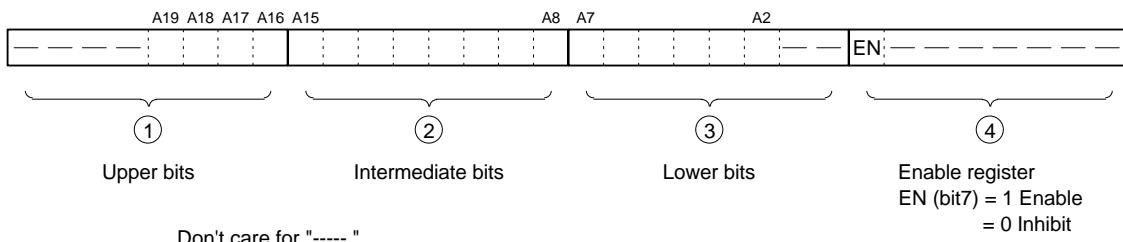


Fig. 6-3

Each BAR is composed of 4 byte address. Bit composition is as follows:



< BAR composition >

Fig. 6-4

④ is the enable register. The entry registers of the break address are assigned to ①, ②, and ③. Each bit of address corresponds to each bit position, writing to ①, ②, and ③ is performed without shifting. The corresponding area is 1MB space of ROS1 and ROS2.

3) SSP register access method

Access to SSP break address register is performed through the temporary register as shown below:

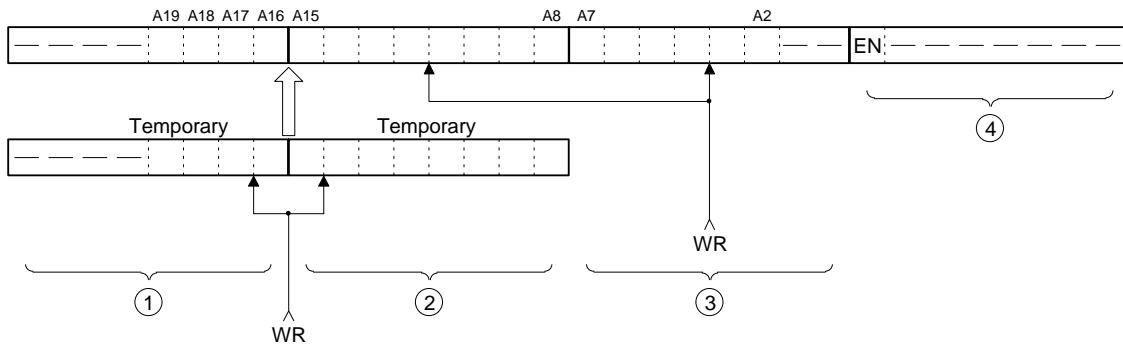


Fig. 6-5

Enable flags can be accessed individually.

Though enable register ④ can be accessed individually, writing to brake address registers ① and ② is performed at the same time as writing to brake address register ③ through the temporary register. Therefore, set ① and ② to temporary, then write into ③ at last. Since the temporary register is commonly used by BAR sets, the following register setting is performed after completion offsetting of each break address register.

③ SSP control method

Access to the enable register and the brake address register is only possible when writing to them from the CPU.

bit 7	6	5	4	3	2	1	0	
0	0	0	CMP4	CMP3	CMP2	CMP1	CMP0	(FFFFFFFFFFH)

← →

Information on which brake register the SSP brake is detected in is read as binary data by reading address FFFFFFFH (*1).

Used in an expanded register.

Normally is a reserve bit. When reading, fixed to 0.

If there are 32 break registers, binary expression is made with the above 5 bits, and 0th is "00000B" and 31st is "11111B."

When detected simultaneously by two or more break registers, one with the smaller BAR number is read as binary data.

The brake signals (NMI) and the above detection data (CMP0~4) are held until the above detection data are read. So read should be made in the NMI sub routine. (Clear by FFFFFFFH read.)

* 1: FFFFFFFH is not full decoded. (FFFF00H~FFFFFFH). Therefore, unnecessary read access in parentheses should not be performed.

7. PRINTER control circuit

1) Block diagram

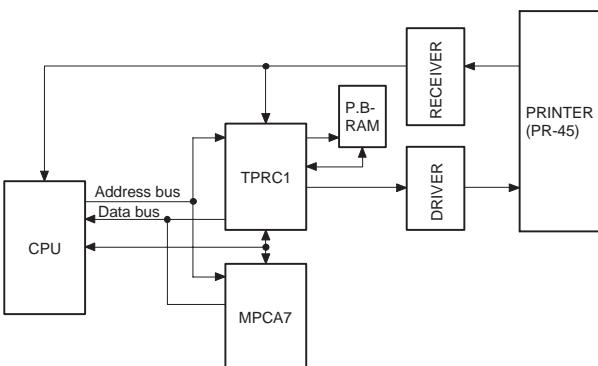
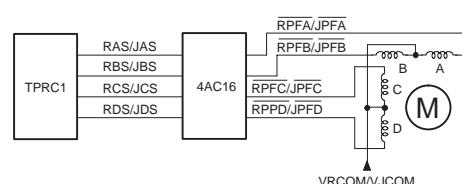


Fig. 7-1

- The thermal printer (PR-45M) is controlled by the thermal printer controller (TPRC1). The PB-RAM connected to TPRC1 serves as a print data buffer.

2) Paper feed circuit



- A pulse motor is used as the paper feed motor.
- Drive sequence of the pulse motor is as follows:

Receipt feed motor: The motor rotates counterclockwise.

Step No.	Phase			
	A	B	C	D
1	ON	OFF	ON	OFF
2	ON	OFF	OFF	ON
3	OFF	ON	OFF	ON
4	OFF	ON	ON	OFF

Journal feed motor: The motor rotates clockwise.

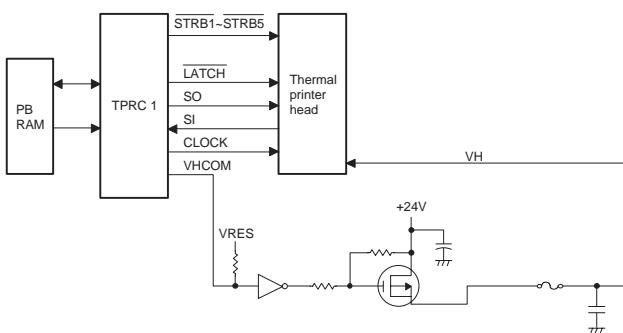
Step No.	Phase			
	A	B	C	D
1	ON	OFF	OFF	ON
2	ON	OFF	ON	OFF
3	OFF	ON	ON	OFF
4	OFF	ON	OFF	ON

Note 1: ON = Conducting
OFF = Not conducting

Note 2: Step No. is performed by the internal process of TPRC1.

- When the motor is locked, the circuit is connected to the CPU through MPCA6.

3) Print circuit



8. Drawer drive circuit

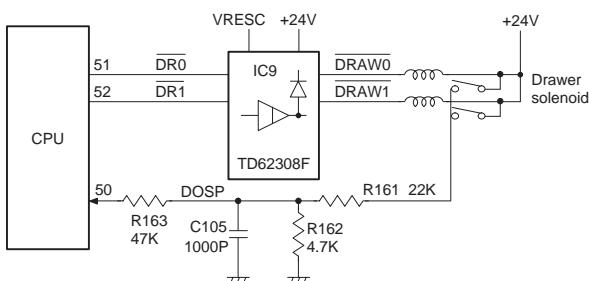


Fig. 8-1

The drawer is directly supported by the CPU. No action starts when the power supply is not steady as the output stage of the driver is pulled VP by VRESC signal.

Drawer open and close is sensed with the microswitch provided in the drawer whose signal is level converted with R161 and R162 and directly read by the CPU.

9. Key, display, time buzzer controls

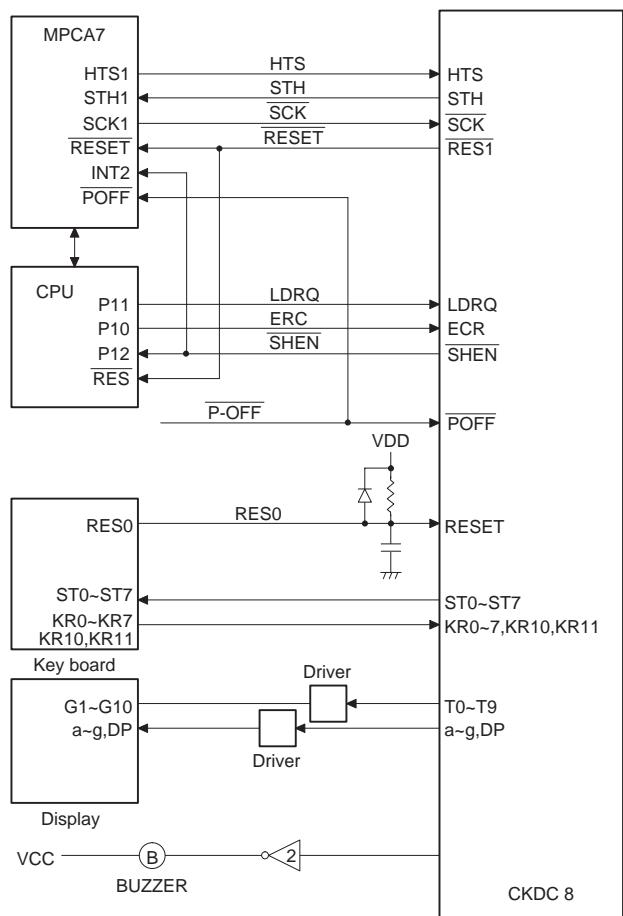


Fig. 9-1

1) Power on sequence

During service interruption, the CKDC8 senses POF within 500msec. When service interruption is cancelled by turning on the power, the CKDC8 cancels resetting of the CPU in the command mode. After initializing each port, the CPU reads the start condition (1 byte).

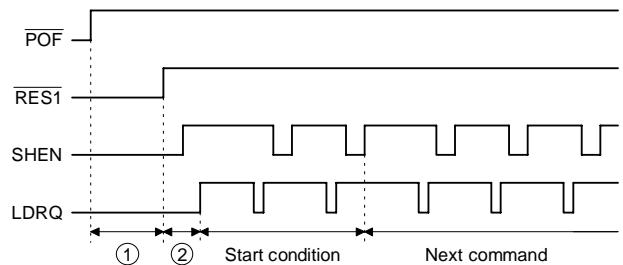


Fig. 9-2

After sampling POF High, the CKDC8 performs mode scan and key scan at ①, then cancels resetting of the CPU. After being cancelled, the CPU initializes each port at ② and reads the start condition.

After being cancelled, the CPU reads the start condition without fail to set the shift mode. If, however, the first starting is made in other than SRV mode after the CKDC8 resets the CPU without request from the CPU, the CKDC8 sets the start condition supposing that starting is made in SRV mode.

2) Power off sequence

When the CPU senses a service interruption, it performs necessary procedures for CPU stop. Then the CPU outputs a reset request to the CKDC8.

Reset request

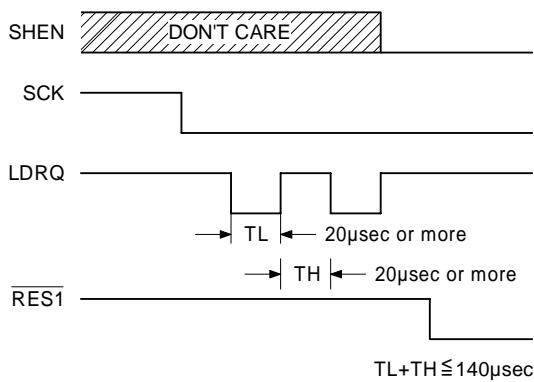


Fig. 9-3

When the CPU senses a service interruption or an error, it performs necessary procedure for CPU stop and issues reset request.

CPU procedures necessary for reset request

- ① All CPU interrupts are made DI.
- ② SCK is driven to low.
- ③ Keep LDRQ at LOW level for 20usec or more and drive it HIGH.
- ④ Loop ① to ③. During looping, access should not be made to external memory.
- ⑤ It should be within 140usec from rising of one LDRQ to rising of another.

When, however, the CKDC8 senses a service interruption at POF, it stops displaying. Service interruption procedure is performed after receiving reset request from the CPU. If reset request is not sent from the CPU within 100msec the service interruption procedure is started after 110 ± 10 msec to go into the stand-by mode.

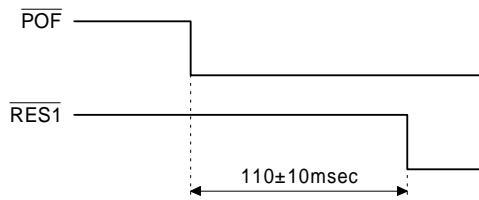


Fig. 9-4

3) Key and switch scanning

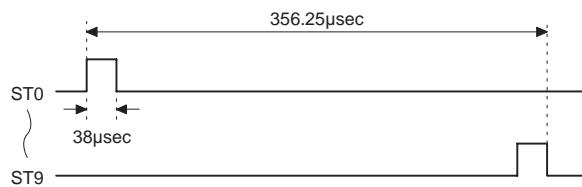


Fig. 9-5

As the strobe signal, 8 bits of ST0 - 8 are used.

KR0 - KR7 are used as the key return signal. KR10 is used as the return signal of the paper feed key, cashier key and MRS switch. KR11 is used as the return signal of the mode switch.

4) DISPLAY CONTROL

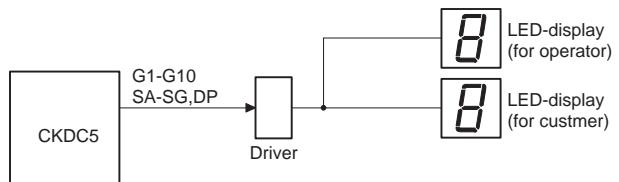


Fig. 9-6

CKDC8 directly drives the LED display unit.

10. Power supply circuit

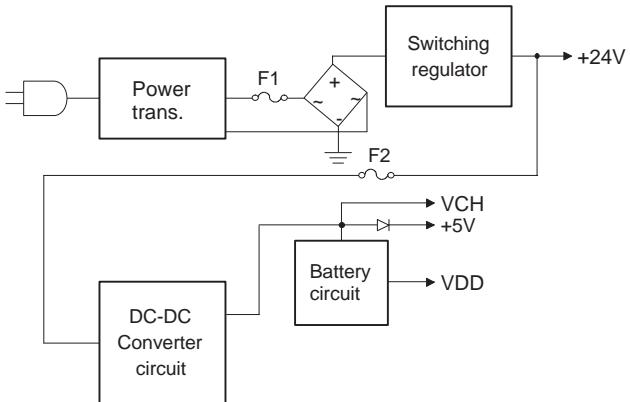


Fig. 10-1

+24V: Printer, solenoid power

+5V: VCC (Logic power)

VDD: Battery charge, Battery back-uped power, CKDC-8 Back-up power

VCH: Fiscal memory unit

CHAPTER 5. TEST FUNCTION

1. General

- 1) This diagnostic program has been developed for diagnosing machine functions in the field. The program is contained within the ER-A450S.

The diagnostic program is stored in the external ROM which will be executed by the CPU (H8/510) which requires the following diagnostic operations:

- Proper power supply voltages are mandatory for logic circuits (+5V, VDD, POFF, +12.5V, +24V).
- CPU input/output pins, CPU internal logic, CKDC8, MPCA7, system bus and common ROM/RAM must be working properly.

2. Operational procedure

To start the diagnostic program, you must enter the following command.

3-digit test item number → key in the SRV mode.

The key assignment must be properly set and the ROM and RAM must be operating properly to go into this mode. This is necessary because the control jumps to the program area in the SRV mode. A master reset must be performed before operating the ECR for the first time. After any option is installed, a program reset is required. When the master reset or program reset is performed, be sure to check the printout on the journal paper.

Master reset: Turn power on in the SRV' mode and change it to the SRV mode with the **JF** key pressed.

Journal print: MASTER RESET ***

Program reset: Turn power on in the SRV' mode and change it to the SRV mode.

Journal print: PRG. RESET ***

3. Test command list

With the SRV mode and the following test code entry, the test start.

CODE	DESCRIPTION
100	Display & Buzzer test
101	Key code & Cashier key test
102	R/J printer test
104	Keyboard test
105	Mode switch test
106	Printer sensor test
108	Calendar oscillator test
109	SSP test
110	Drawer open sensor test (For standard drawer)
111	Drawer open sensor test (For remote drawer)
120	Standard RAM test
130	Standard ROM test
150	Printer dot pulse width adjustment
200	Option RAM test
501	RS-232 channel 1 Loop back check
550	RS-232 channel 8 Loop back check

4. Test contents

[1] Display & Buzzer test

1) Key operation

100 → **TL**

2) Functional description

Display the following message on the front and the rear display boards.

1. 2. 3. 4. 5. 6. 7. 8. 9. 0.

A decimal point shifts from lower number of digit by one digit (per 200m sec.).

Next, display the following segments (for approx. 1 sec.).

8. 8. 8. 8. 8. 8. 8. 8. 8.

Repeat the above two kinds of displays.

Sound a buzzer continuously during test.

3) Check items

- The display must be correctly shown at each position.
- The luminosity of displays must be uniform and even at each position.
- Abnormal buzzer sound is not allowed.

4) Test termination

Press any key. The test terminates with the test and message printed

1 0 0

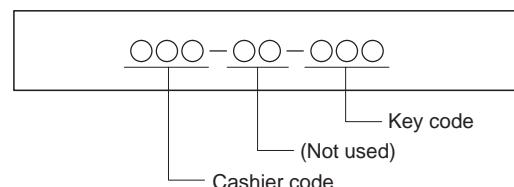
[2] Key code & Cashier key test

1) Key operation

101 → **TL**

2) Functional description

Key code, MRS switch state and Cashier code are displayed.



3) Check items

- a) Cashier code (One hole cashier key: OPTION)

Display	State
000	Off
001	Cashier key No.1
002	Cashier key No.2
003	Cashier key No.3
↓	↓
014	Cashier key No.14
015	Cashier key No.15

- b) Key code

HARDWARE CODE" of the following keys will be displayed every time the keys are pressed.

"--" indicates that a key is struck twice and also that input data is not accepted.

[KEY POSITION CODE]

<ALL KEY>

										65	68	67	58	77	78
										66	55	56	57	48	38
R	J	63	62	61	52	51	60	40	45	35	46	47	37		
74	43	33	42	32	41	31	49	30	76	75	36	28	27		
14	23	24	22	72	21	71	20	70	15	05	16	17	18		
04	13	03	12	02	11	01	10	00	26	25	06	07	08		

<ER-A450S STANDARD KEY BOARD LAYOUT>

										65	68	67	58	77	78
										66	55	56	57	48	38
R	J	63	62	61	52	51		40	45	35	46	47	37		
74	43	33	42	32	41	31		30	76	75	36	28	27		
14	23	24	22	72	21	71		70	15	05	16		18		
04	13	03	12	02	11	01		00	26	25	06		08		

4) Test termination

Change the mode switch position other than SRV position to terminate the test.

The test terminates with the test and message printed

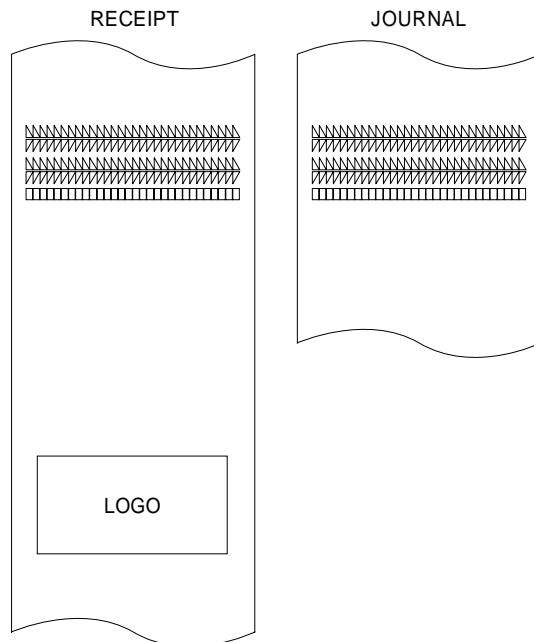
1 0 1

[3] R/J printer test**1) Key operation**

102 → TL

2) Functional description

Five lines of special characters are printed as follows on the receipt and the journal regardless of receipt (ON/OFF) switch setting.

**3) Check items**

- Check that the slanted lines of special characters are clearly printed.
- Check that the characters are printed at a uniform density.
- Check the paper feed operation and the logo print.

4) Test termination

This check is terminated automatically.
The termination print is not performed.

[4] Keyboard test**1) Key operation**

XXXX 104 → TL

XXXX: Sumcheck data

Standard keyboard layout sumcheck data	
ER-A450S	2314

2) Functional description

Keyboard test is performed with the sumcheck data of key code. For sumcheck data, data are inputted to the upper four digits before the diagnostics code.

The data are compared with the added data which are added until the final key (TL) is pressed. If the data agree with the added data, the end print is made. If not, the error print is made.

The sum check data is obtained by totaling all key hardware codes except for the (TL) key and converting the total into a decimal figure.

[ALL KEY LAYOUT]

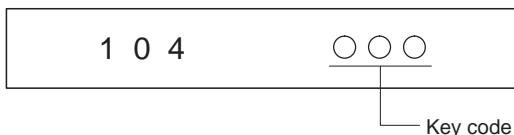
					41	44	43	3A	4D	4E
					42	37	38	39	30	26
R	J	3F	3E	3D	34	33	3C	28	2D	23
A4	2B	21	2A	20	29	1F	32	1E	4C	4B
0E	17	18	16	48	15	47	14	46	0F	05
04	0D	03	0C	02	0B	01	0A	00	1A	19
									06	07
									08	

[STANDARD KEYBOARD LAYOUT]

SUMCHECK DATA = A4 + 0E + 04 + 2B + 17 + = 2243

		44		43	3A	4D	4E
R	J	3F	3E	3D	34	33	
A4	2B	21	2A	20	29	1F	
0E	17	18	16	48	15	47	
04	0D	03	0C	02	0B	01	
				00	1A	19	06
							08
				42	37	38	39
					30	26	
				28	2D	23	2E
					2F	25	

Display the following message on the front display.

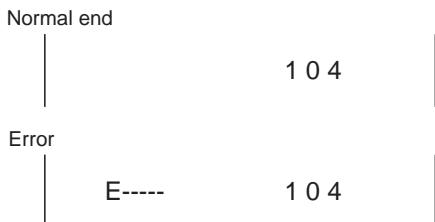
**3) Check items**

- a) Check of the display in the test and the content of end print.

4) Test termination

This check is terminated automatically.

The test terminates with the test and message printed

**[5] Mode switch test****1) Key operation**

105 → TL

2) Functional description

Display the following message on the front display.



When the Mode Switch is switched over in the following order, a numerical value corresponding to each position of mode switch is displayed at X.

Mode: SRV → PGM2 → PGM1 → OFF → OP X/Z

x : 0 → 1 → 2 → 9 → 3

SRV ← X2/Z2 ← X1/Z1 ← MGR ← REG ←

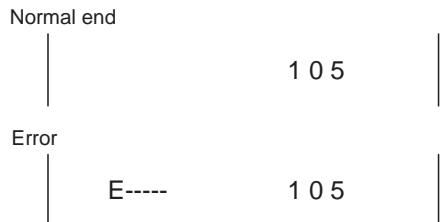
0 ← 7 ← 6 ← 5 ← 4 ←

3) Check items

- a) Check of the display in the test and the content of end print.

4) Test termination

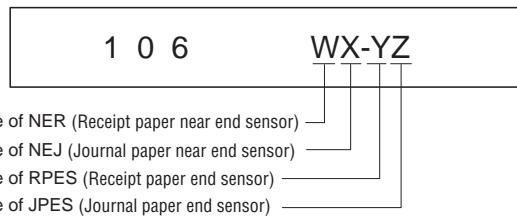
The test terminates with the test and message printed

**[6] Printer sensor test****1) Key operation**

106 → TL

2) Functional description

State of the paper near end sensor is sensed and displayed.

**3) Check items**

	Displayed	Description
W (NER)	0	Receipt paper near end sensor: Detected
	1	Receipt paper near end sensor: Not detected
X (NEJ)	0	Journal paper near end sensor: Detected
	1	Journal paper near end sensor: Not detected
Y (RPES)	0	Receipt paper end sensor: Detected
	1	Receipt paper end sensor: Not detected
Z (JPES)	0	Journal paper end sensor: Detected
	1	Journal paper end sensor: Not detected

* "1" is always display when no sensor is used.

4) Test termination

Press any key. The test terminates with the test and message printed



[7] Calendar oscillator test**1) Key operation**108 → **2) Functional description**

This program is used to test the calendar oscillator function.

Display:

"** - **" shows the current time.

"-" is blinking. (500ms ON and OFF)

3) Check items

Time elapsed after master reset must be displayed.

4) Test termination

Press any key. The terminates with the test and message printed

[8] SSP test**1) Key operation**109 → **2) Functional description**

If an SSP is programmed, its contents are automatically checked and the result is printed.

Display:

3) Check items

Check printing of the termination message.

4) Test termination

This check is terminated automatically.

The test terminates with the test and message printed

Normal end

Error

E-----

SSP table full

F-----

* In this SSP check, set the data for check in the empty area of SSP entry REG and erase the data for check after completion of check. Therefore SSP setting before check is not cleared.

If therefore there is no SSP entry REG remained for SSP check, F-print is performed to terminate the program without check.

[9] Drawer open sensor test (For standard test)**1) Key operation**110 → **2) Functional description**

State of the drawer open sensor is sensed and displayed.

3) Check items

X	Description
O	Drawer open sensor detected. (Drawer open)
C	Drawer open sensor not detected. (Drawer closed)

a) Check opening of the specified drawer.

b) Check the display indication when the drawer is open and closed.

4) Test termination

Press any key. The test terminates with the test and message printed

[10] Drawer open sensor test (For remote drawer)**1) Key operation**111 → **2) Functional description**

State of the drawer open sensor is sensed and displayed.

3) Check items

X	Description
O	Drawer open sensor detected. (Drawer open)
C	Drawer open sensor not detected. (Drawer closed)

a) Check opening of the specified drawer.

b) Check the display indication when the drawer is open and closed.

4) Test termination

Press any key. The test terminates with the test and message printed

[11] Standard RAM test**1) Key operation**120 →

2) Functional description

Perform the following check for the standard RAM 256 KByte SRAM. The memory contents should not be changed before and after the check.

Perform the following processes for memory address to be checked (1C0000H~1FFFFFH).

PASS1: Save memory data.

PASS2: Write data "0000H."

PASS3: Read and compare data "0000H," write data "5555H."

PASS4: Read and compare data "5555H," write data "AAAAH."

PASS5: Read and compare data "AAAAH."

PASS6: Restore the memory data.

If a compare error occurs in the check sequence PASS1-PASS6, an error print is made. If no error occurs through all address, the check ends normally.

The following address check is performed further.

Check point address =

1C0000H, 1C0001H, 1C0002H, 1C0004H
1C0008H, 1C0010H, 1C0020H, 1C0040H
1C0080H, 1C0100H, 1C0200H, 1C0400H
1C0800H, 1C1000H, 1C2000H, 1C4000H
1C8000H, 1D0000H, 1E0000H, 1F0000H

7-SEGMENT DISPLAY: 1 2 0

3) Check the following items:

Check the termination printout.

4) Test termination

The test terminates after printing the termination printout.

Termination printout:

Normal termination	120
Abnormal termination	Ex -----
	120

X =	1: Data check error
	2: Address check error

Note: When an error occurs, the error print is performed and the check is terminated. The error occurrence address is shown in hexadecimal at positions shown with *****.

[12] Standard ROM test

1) Key operation

130 → TL

2) Functional description

Sum check of the standard ROM (C0000H - C7FFFFH) is performed. If the lower two digits of SUM is 10H, it is normal.

7-SEGMENT DISPLAY: 1 3 0

3) Check the following items:

Check the printout after the test.

4) Test termination

The test automatically terminates with termination message.

Normal termination print	130
ROM1	<u>27040*****</u>

Error termination print	E -----
ROM1	27040*****

Note: "*****" means the ROM version number.

The underlined section (10 bytes) of code table is provided in the ROM as a standard and the table content is always printed.

The table position is the upper 10 digits of the ROM address. The check sum correction address is the last address -0FH.

[13] A/D conversion test

1) Key operation

151 → TL

2) Contents

The digital conversion value of the input signal to the CPU A/D converter is displayed sequentially. The display channel is changes is approx. 1 sec. interval by timer control and is displayed repeatedly.

Thermistor input

7-SEGMENT DISPLAY:	1 5 1 1 XXXX
--------------------	------------------------

Vrf input: Vrf means the presumed voltage of VRF when VCC is supposed to be +0.5V.

7-SEGMENT DISPLAY:	1 5 1 2 XXXX
--------------------	------------------------

+24V input

7-SEGMENT DISPLAY:	1 5 1 3 XXXX
--------------------	------------------------

Head input

7-SEGMENT DISPLAY:	1 5 1 4 XXXX
--------------------	------------------------

Note: "XXXX": The 10 bit data of the A/D convertor displayed in decimal number.

Therefore, its connect may be 0000 ~ 1024.

3) Confirmation

Check the display content.

4) Termination

To when the mode switch is set to any mode other than SRV mode, the termination print is made and the test is terminated.

151
Test termination print

[14] Option RAM test

1) Key operation

200 → TL

JOB #NO.	RAM NO.	Memory to be checked	Address area to be checked
200	Option RAM	ER-03RA	200000H ~ 27FFFFH

2) Content

The following check are performed for the optional RAM.

The following process is performed for memory addresses to be checked.

PASS1: memory data save

PASS2: Data "0000H" write

PASS3: Data "0000H" read and comparison, data "5555H" write

PASS4: Data "5555H" read and comparison, data "AAAAH" write

PASS5: Data "AAAAH" read and comparison

PASS6: Memory data restore

If a compare error is found in the check sequence from PASS1 to PASS6, error print (error code E1) is performed. If there is no error found to the end of the last address, the operation is completed normally.

Then the following address check is performed. "O" shows a valid address, and "X" shows an invalid address.

In case of an error, error code E2 is printed.

Check Address	JOB#201(ER-03RA)
200000H	
200001H	
200002H	
200004H	
200008H	
200010H	
200020H	
200040H	
200080H	
200100H	
200200H	
200400H	
200800H	
201000H	
202000H	
204000H	
208000H	
210000H	
220000H	
240000H	
260000H	

7 SEGMENT DISPLAY: 2 0 0

3) Check the following items.

Check the termination print.

4) Test termination

The test terminates after printing the termination printout.

Termination print

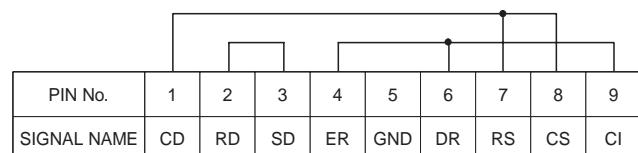
E1---	200	(data check error)
E2---	200	(address check error)

	200	(normal end)

*****: Error address

[15] RS-232 Channel 1 check**[16] RS-232 channel 8 check**

Loop back connector for D-SUB 9pin : UKOG-6705RCZZ

**1) Key operation check**

The program is activated by JOB#501 or JOB#550

SRV mode: 501 → : Channel 1

550 → : Channel 8

2) Functional descriptiton

If the channel specified by JOB#CODE is not set, the machine performs the mis-operation processing. When the channel is set, the machine conducts the loop check concerning the channel specified by JOB#CODE by using the loopback connector.

The following three items are checked:

- ① Control signal check
- ② Data transfer check
- ③ Timer check (RS-232 onboard timer)

Check ①

Control signal check (\overline{ERn} - \overline{DRn} - \overline{CIn} , \overline{RSn} - \overline{CDn} - \overline{CSn} loop check)

OUTPUT		INPUT			
\overline{ERn}	\overline{RSn}	\overline{DRn}	\overline{CIn}	\overline{CDn}	\overline{CSn}
OFF	OFF	OFF	OFF	OFF	OFF
OFF	ON	OFF	OFF	ON	ON
ON	OFF	ON	ON	OFF	OFF
ON	ON	ON	ON	ON	ON

The read check about the above INPUT items and interrupt check of \overline{CS} , \overline{CI} and \overline{CD} are performed.

Read check: \overline{ER} and \overline{RS} are switched over in the order as shown in the above table to confirm the logic of DR, CI, CD and CS. If the read logic is different from the one in the table, error print-outs occur.

Interrupt check: Allows the interruption of either of \overline{CS} , \overline{CI} and \overline{CD} one by one. (The mask is released.)

The interruption does not take place when each signal is turned on. Or if the interruption occurs when a signal is turned off, error print-outs occur.

Each of the above checks should be made in four cycles.

Check ② Data transfer check (SDn-RDn loop check)

In this check, transfer 256-byte loopback data of \$00~\$FF.

Note) The above check should be made with the baud rate set at 9600BPS.

Check ③ Timer check

Before making check ②, set the corresponding timer at 10ms for RCVDT activation, and check to see that:

- 1) $\overline{TRQ1}$ is not generated during the execution of check ②.
- 2) $\overline{TRQ1}$ is generated in 10msec. after check ② is finished.

3) Check the followin item

If an error occurs during the above checks, following error print-outs occur. Even if an error occurs during check ①, the test is continued after the corresponding error print-out has occurred, but if an error occurs during the execution of check ② or ③, the test is terminated after the corresponding error print-out has occurred.

Note that when check ①, ② or ③ terminates, the termination print-

out occurs irrespective of any errors that have occurred during the check. (The program terminates normally only when no error print-out has occurred.)

ERROR	ERROR PRINT	Contents
1	E1-ER DR	ERn-DRn ERR
2	E2-ER CI	ERn-CIn ERR
3	E3-RS CD	RSn-CDn ERR
4	E4-RS CS	RSn-CSn ERR
5	E5-CI INT	Interruption error of CIn
6	E6-CD INT	Interruption error of CDn
7	E7-CS INT	Interruption error of CSn
8	E8-TXEMP	TXEMPn error
9	E9-TXEMP I	Interruption error of TXEMPn
10	E10-TXRDY	TXRDYn error
11	E11-TXRDY I	Interruption error of TXRDYn
12	E12-RCVRDY	RCVRDYN error (Reception is impossible. TRQ1 has occurred during execution of check ②.)
13	E13-RCVRDY I	Interruption error of RCVRDY
14	E14-SD RD	SDn-RDn ERR (Data error)
15	E15-SD RD	SDn-RDn ERR (Data error, Flaming error)
16	E16-TIMER	TIMERn error (TMRQn cannot be set after termination of check ②.)
17	E17-TIMER I	Interruption error of TRQ1

Errors that may occur during check ① (control signal check): E1~ E7

Errors that may occur during check ② (data transfer check): E8~ E15

Errors that may occur during check ③ (timer check): E12, E16 and E17

4) Test termination

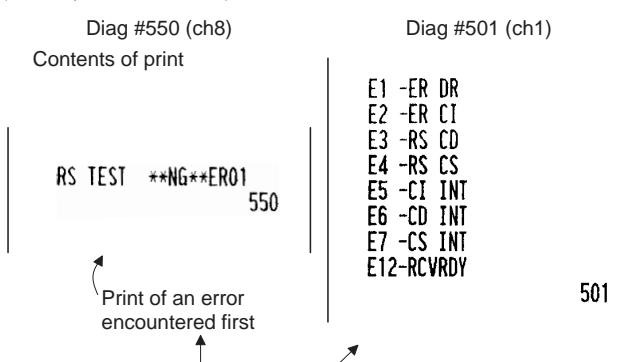
The program automatically terminates when a check is finished.

Termination print-out:

50nn nn : 01 or 50

Ref.:Print generated when an error occurs

When no communication is established:
(w/o loopback connector)



The contents of prints are different even if the error is the same.

CHAPTER 6. DOWN LOAD FUNCTION

1. General

RAM data can be transmitted in the following two methods.

Save the data before servicing as follows:

① ECR ↔ ECR

- Cable: 9 pin D-SUB – 9 pin D-SUB



Fig. 1-1

② ECR ↔ ER-02FD

- Cable: 9 pin D-SUB – 25 pin D-SUB



Fig. 1-2

2. SIO interface specification

- 1) Operation: Simplex
- 2) Line configuration: Direct connect
- 3) Data rate: 19200, 9600, 4800, 2400, 1200, 600, 300BPS (Selected by SRV JOB#903-A)
- 4) Sync mode: Asynchronous
- 5) Checking: Vertical parity (odd)
- 6) Code: 7 bits (ASCII)
- 7) Bit sequence: LSB first
- 8) Line level: RS232 level
- 9) Data format:

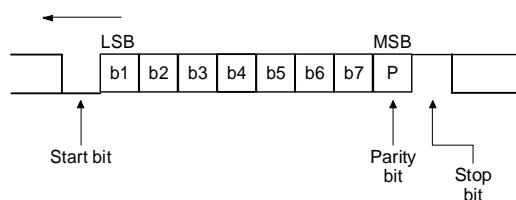


Fig. 2-1

3. Location of connector pins

① ECR-ECR cable



SD : TRANSMITTED DATA

RD : RECEIVED DATA

DTR: DATA TERMINAL READY

DSR: DATA SET READY

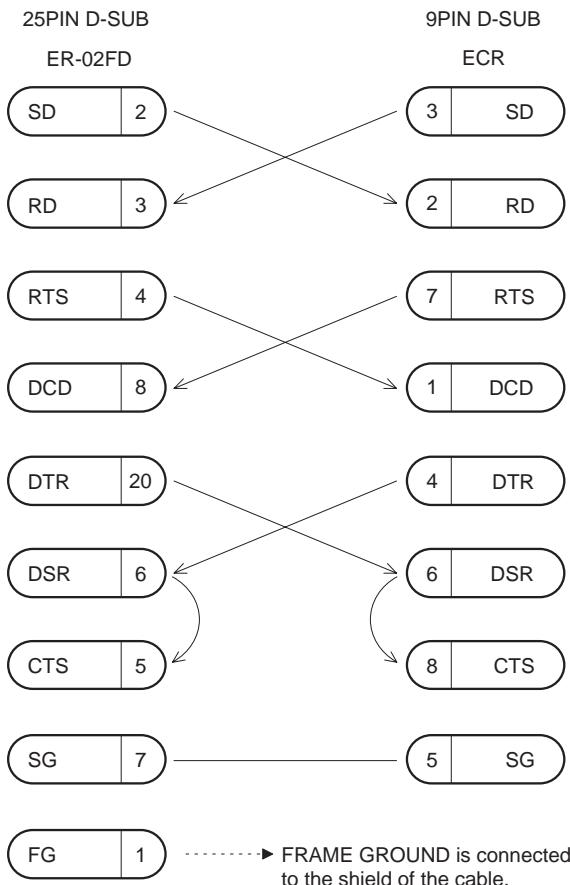
RTS: REQUEST TO SEND

DCD: DATA CARRIER DETECTOR

CTS: CLEAR TO SEND

Fig. 3-1

② ECR-ER-02FD cable



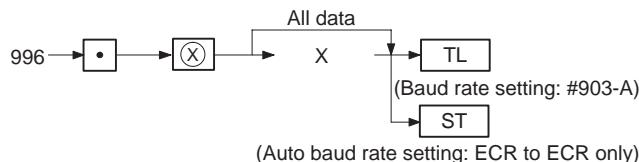
SD : TRANSMITTED DATA
 RD : RECEIVED DATA
 DTR: DATA TERMINAL READY
 DSR: DATA SET READY
 RTS: REQUEST TO SEND
 DCD: DATA CARRIER DETECTOR
 CTS: CLEAR TO SEND
 FG : FRAME GROUND

Fig. 3-2

4. Application specification

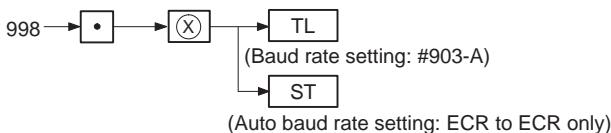
The following service (SRV) modes are available for the serial data transfer of the ECR

1) Data transmit (Source side)



X: 0=SSP DATA

2) Data receive (Target)



5. Data format

A single byte image of the RAM data to be transmitted is divided into a high order 4 bits and low order 4 bits and converted into ASCII code. Then, the image of the memory is sent in the following format:



① Memory top address: 0000H ~ FFFFH
 Top address of the memory to be transmitted in ASCII number.

② Page: 1F ~ 27,000
 Page of the memory to be transmitted in ASCII number.

③ Sum check

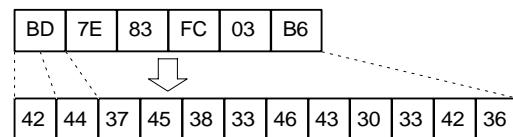
④ End code: Hex 0D

NOTE:

- In order that contents of RAM memory may not over-ride pages for this job, RAM image is sent in unit of 64 bytes from the address 0000. In other words, 128 bytes are sent at one time on the transmit data format.

RAM DATA FORMAT

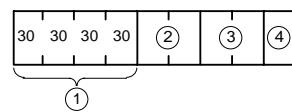
Exhibit:



Code table

HEX	ASCII	Character	HEX	ASCII	Character
0	30	0	8	38	8
1	31	1	9	39	9
2	32	2	A	41	A
3	33	3	B	42	B
4	34	4	C	43	C
5	35	5	D	44	D
6	36	6	E	45	E
7	37	7	F	46	F

6. END record



① End message: Fixed to 30303030.

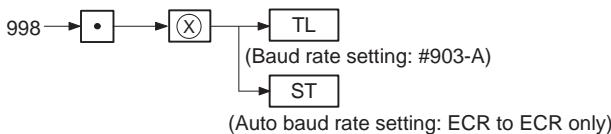
② End message: Fixed to 4646.

③ Sum check

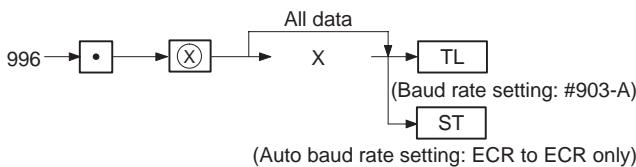
④ End code: CR (0D)

7. Operational method

- 1) To prepare an ECR to receive data from another ECR or the ER-02FD, the memory size of the receiving unit must be the same as or greater than the sending unit.
- 2) Master reset the receiving ECR.
- 3) Connect loader cable between ECRs.
- 4) Set the receiving ECR ready to receive.



- 5) Start the sending ECR.



X: 0 = SSP

- 6) Transmission status.

Description of error status

- 1: Application error (Command error)
 - 2: Application error (Parity error)
 - 3: Application error (Check sum error)
 - 4: Application error (Data size error)
 - 5: Hard ware error
 - 6: Power off error
 - 7: Time out error
 - 11: Application error (Transmit data size error)
 - 12: Application error (Block sequence error)
- 7) Service reset the receiving ECR.

8. Saving/Loading of data to/From the FD unit Configuration

- 1) Turn off the power switch of the ER-02FD, and set the DIP switches of the FD unit as follows:

ER-02FD (The ER-01FD functions of the ER-02FD are used.)

DS-1								DS-2			
1	2	3	4	5	6	7	8	1	2	3	4
OFF	ON	OFF	ON	OFF	OFF	OFF	ON	X	ON	OFF	OFF

Data rate

4	6	Rate [bps]
OFF	OFF	19200
ON	OFF	9600
OFF	ON	4800
ON	ON	2400

Disk format
CCP/M: OFF
PC-DOS: ON

- 2) Connect the cable.

Saving data

- 1) Turn on the power switch and insert a floppy disk which has been formatted.
- 2) Start the SEND JOB on the ECR side as follows:



X: 0 = SSP

- 3) Data transmission is started and the green lamp on the ER-02FD blinks.

Loading data

- 1) Turn on the power switch and insert the floppy disk which stores the data.
- 2) Start the RECEIVE JOB on the ECR side as follows:



- 3) Press the [SEND] key on the FD unit.

- 4) Data transmission is started and the Green lamp on the ER-02FD blinks.

- 5) Service reset the ECR.

CHAPTER 7. SERVICE PRECAUTION

1. Error code table

When the following error codes are displayed, press the / key and take a proper action according to the table below.

Error code	Error status	Action
E01	Registration error	Make a correct key entry.
E02	Misoperation error	Make a correct key entry.
E03	Undefined code is entered.	Enter a correct code, or declare it by the programming.
E04	Paper empty	Replace a journal paper roll with a new one.
E05	Secret code error	Enter a correct secret code.
E07	Memory is full.	Expand the file within a capacity of memory.
E11	Compulsory depression of the) key for direct finalization	Press the) key and continue the operation.
E12	Compulsory tendering	Make a tendering operation.
E22	Overlapped cashier error	
E23	Cashier resetting over error	
E31	Compulsory non-add code entry	Enter a non-add code.
E32	No entry of your cashier code	Make a cashier code entry.
E33	The current cashier code should not be changed.	Change a cashier after finalizing the transaction.
E34	Overflow limitation error	Make a registration within a limit of entry.
E35	The open price entry is inhibited.	Make a preset price entry.
E36	The preset price entry is inhibited.	Make an open price entry.
E37	The direct finalization is inhibited.	Make a tendering operation.
E58	Undefined clerk code is entered	Enter a correct clerk code.
E67	Registration buffer is full.	
E76	The drawer is still opened.	Close the drawer.
E86	Communication error	SRV #996/#998
E87	Data format error	SRV #996/#998
E88	Time-out error	SRV #996/#998

2. Conditions for soldering circuit parts

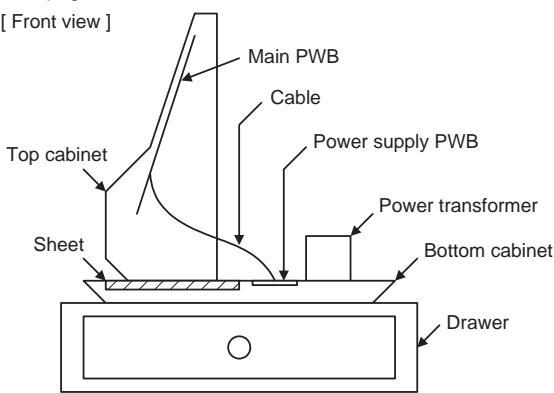
To solder the following parts manually, follow the conditions described below.

PARTS NAME	PARTS CODE	LOCATION	CONDITIONS FOR SOLDERING
Front LED (HDSP5621)	VPHDSP 5 6 2 1 – 1	Front LED PWB: FND1-5	315°C/2 sec.
Pop-up LED (HDSP-F501#S02)	VPHDSPF 5 0 1 – 1	Pop-up LED PWB: FND1-10	315°C/2 sec.

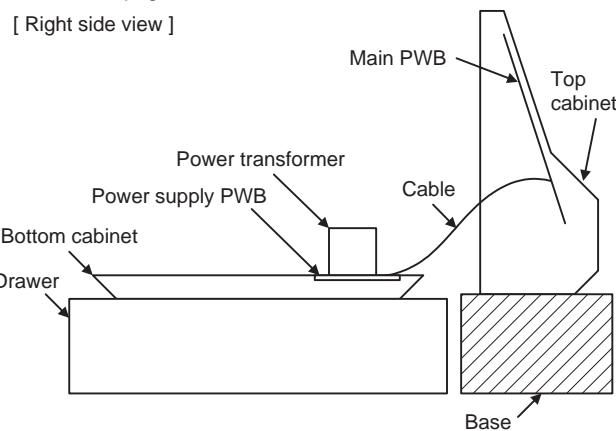
3. Caution to be taken when removing the TOP CABINET

After removing the ER-A450S's TOP CABINET from the BOTTOM CABINET, put the TOP CABINET on the positions given below to prevent the cable that connects the MAIN PWB and POWER SUPPLY PWB from disconnecting.

- 1) Put the TOP CABINET on the left of the BOTTOM CABINET.
Put a sheet on the BOTTOM CABINET and put the TOP CABINET upright on the sheet, as shown below.

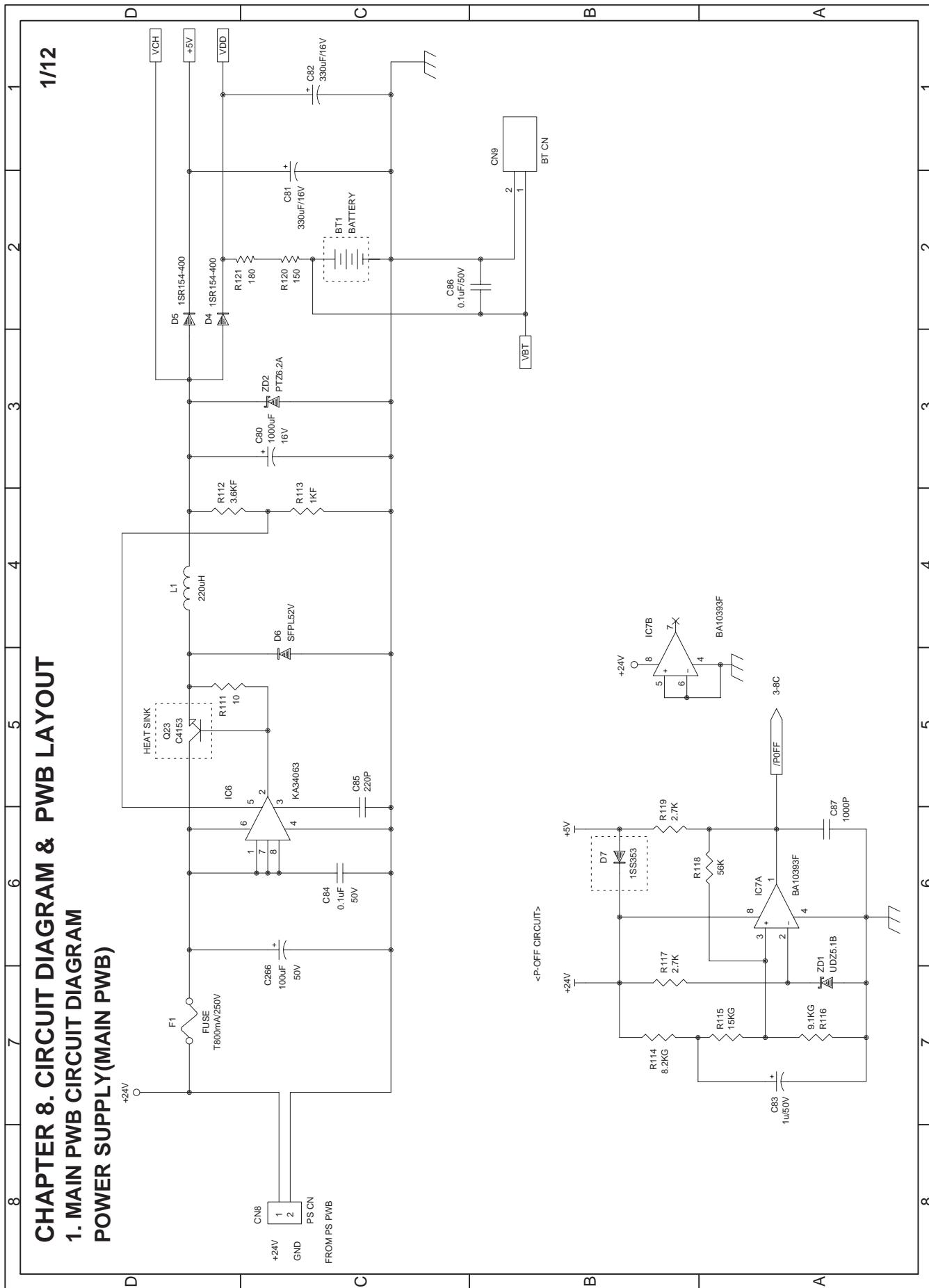


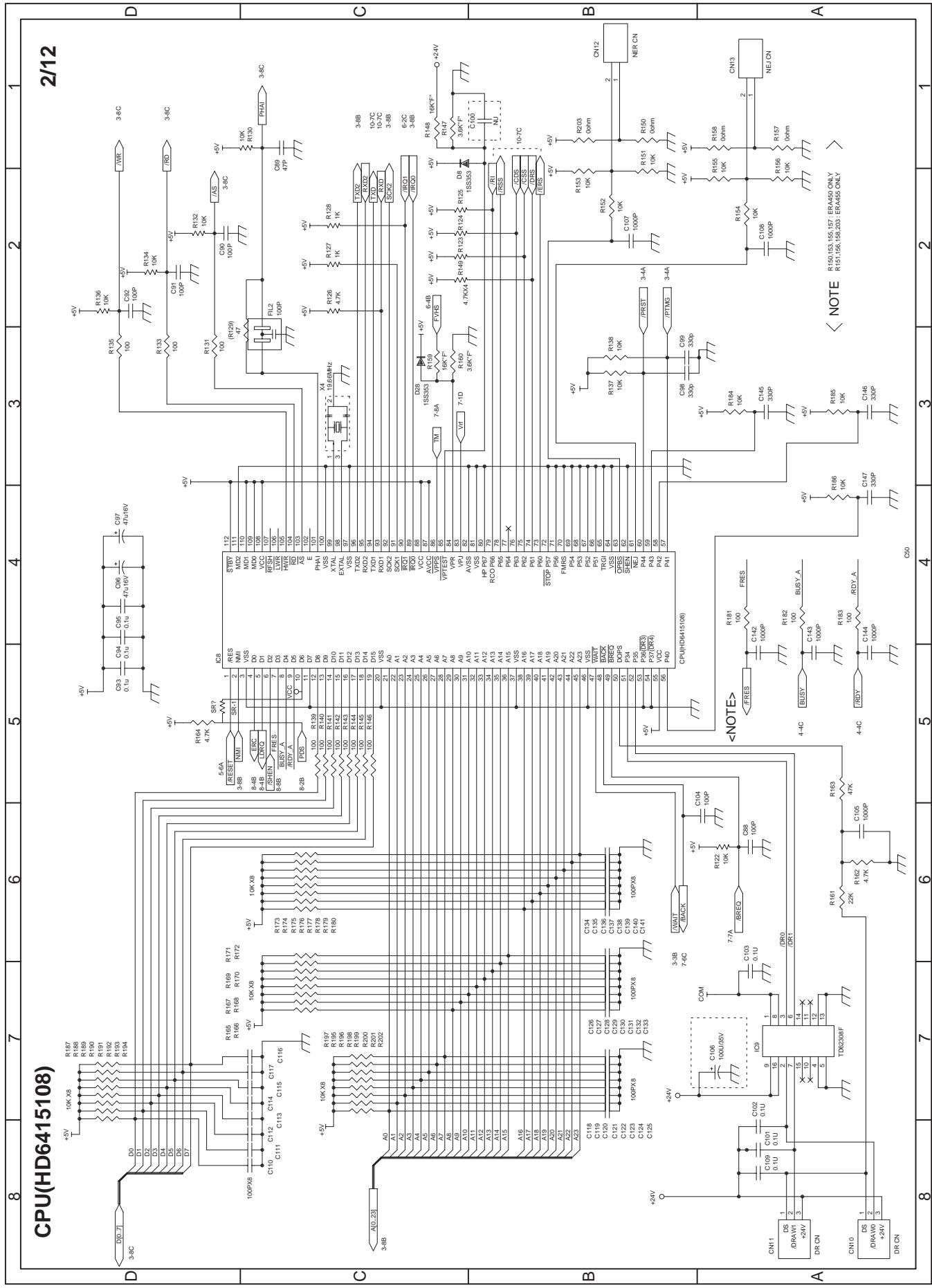
- 2) Put the TOP CABINET behind the drawer
Put a base (proper height) behind the drawer and put the TOP CABINET upright on the base, as shown below.

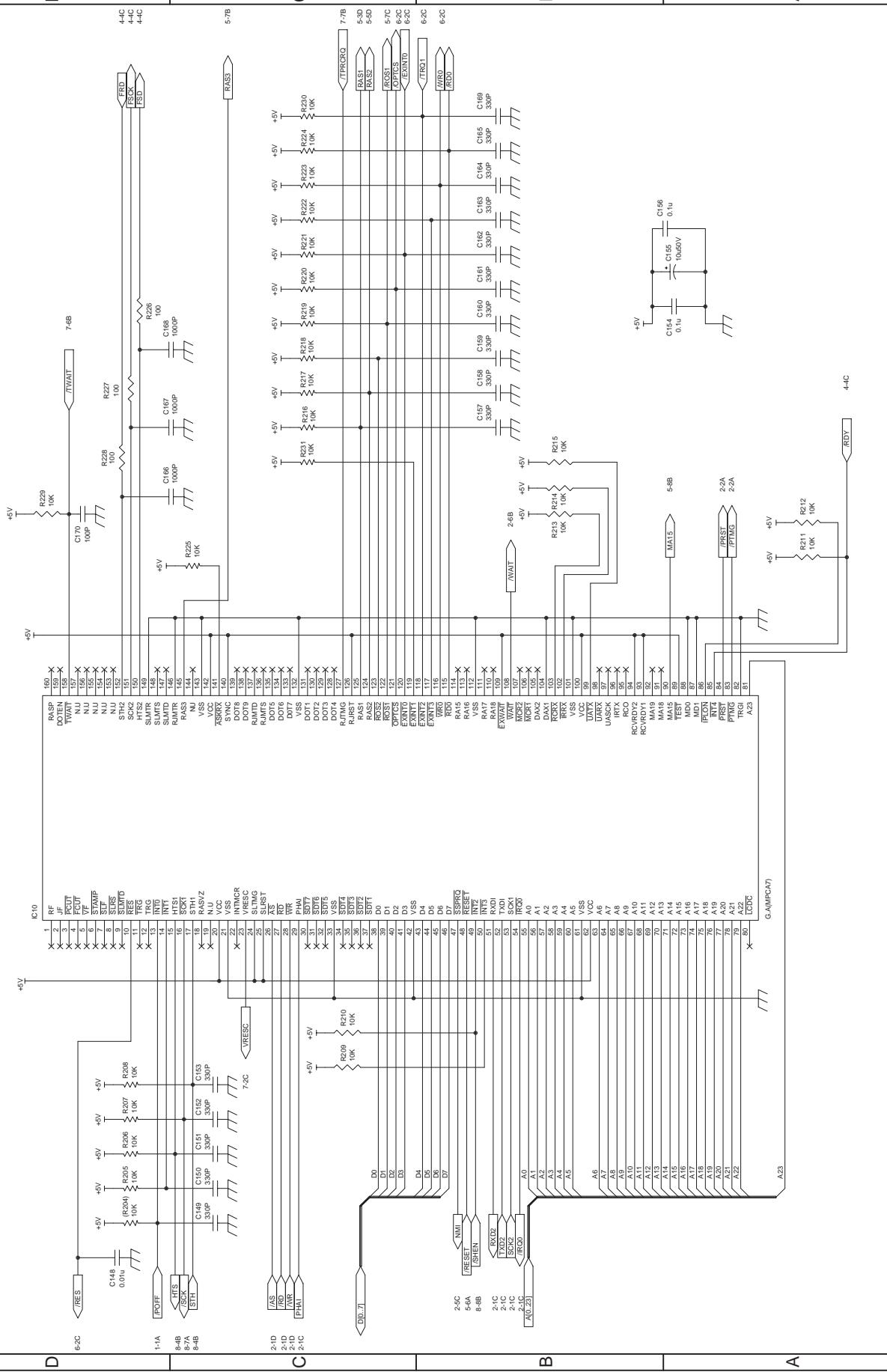


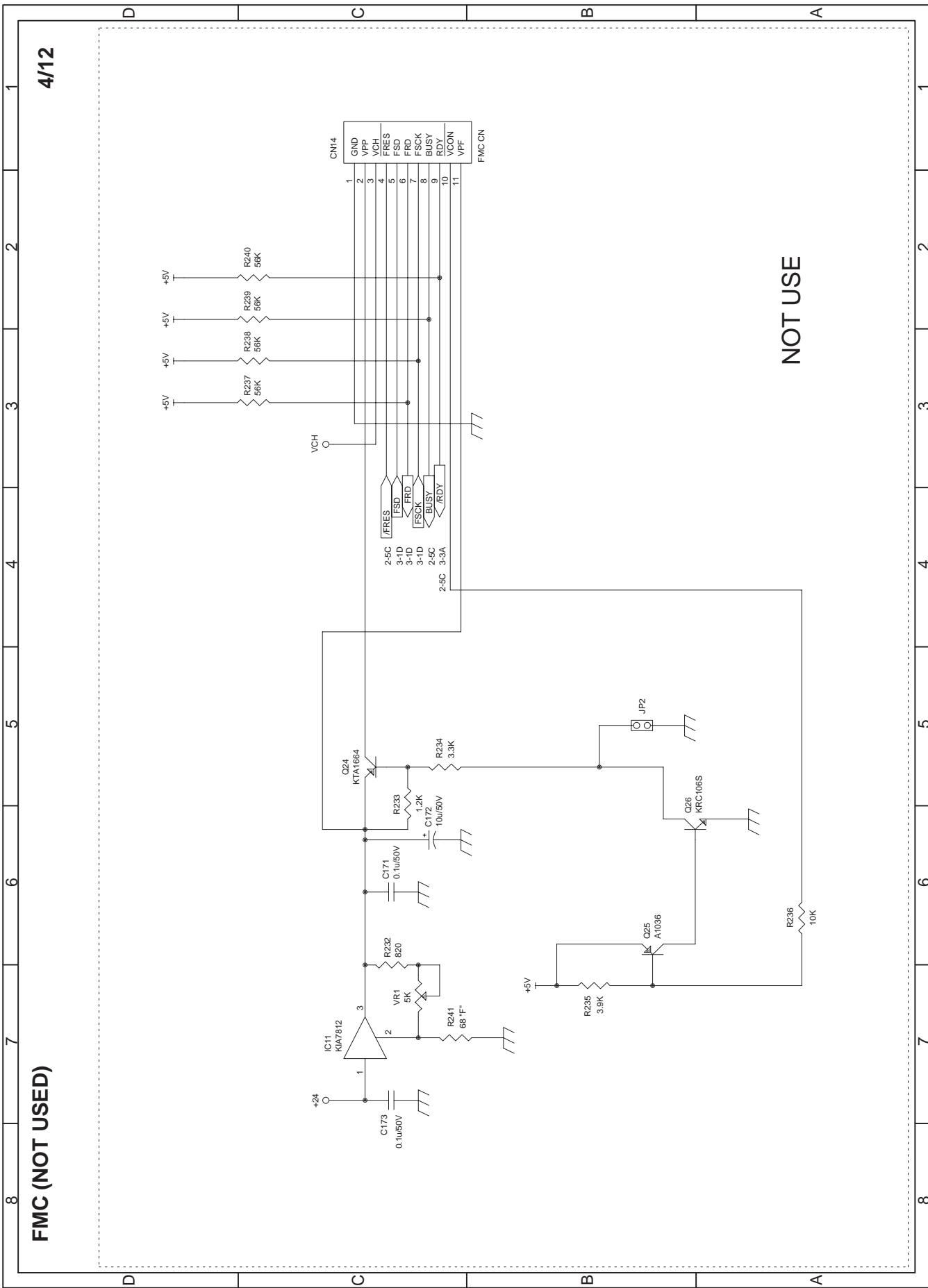
CHAPTER 8. CIRCUIT DIAGRAM & PWB LAYOUT
1. MAIN PWB CIRCUIT DIAGRAM
POWER SUPPLY(MAIN PWB)

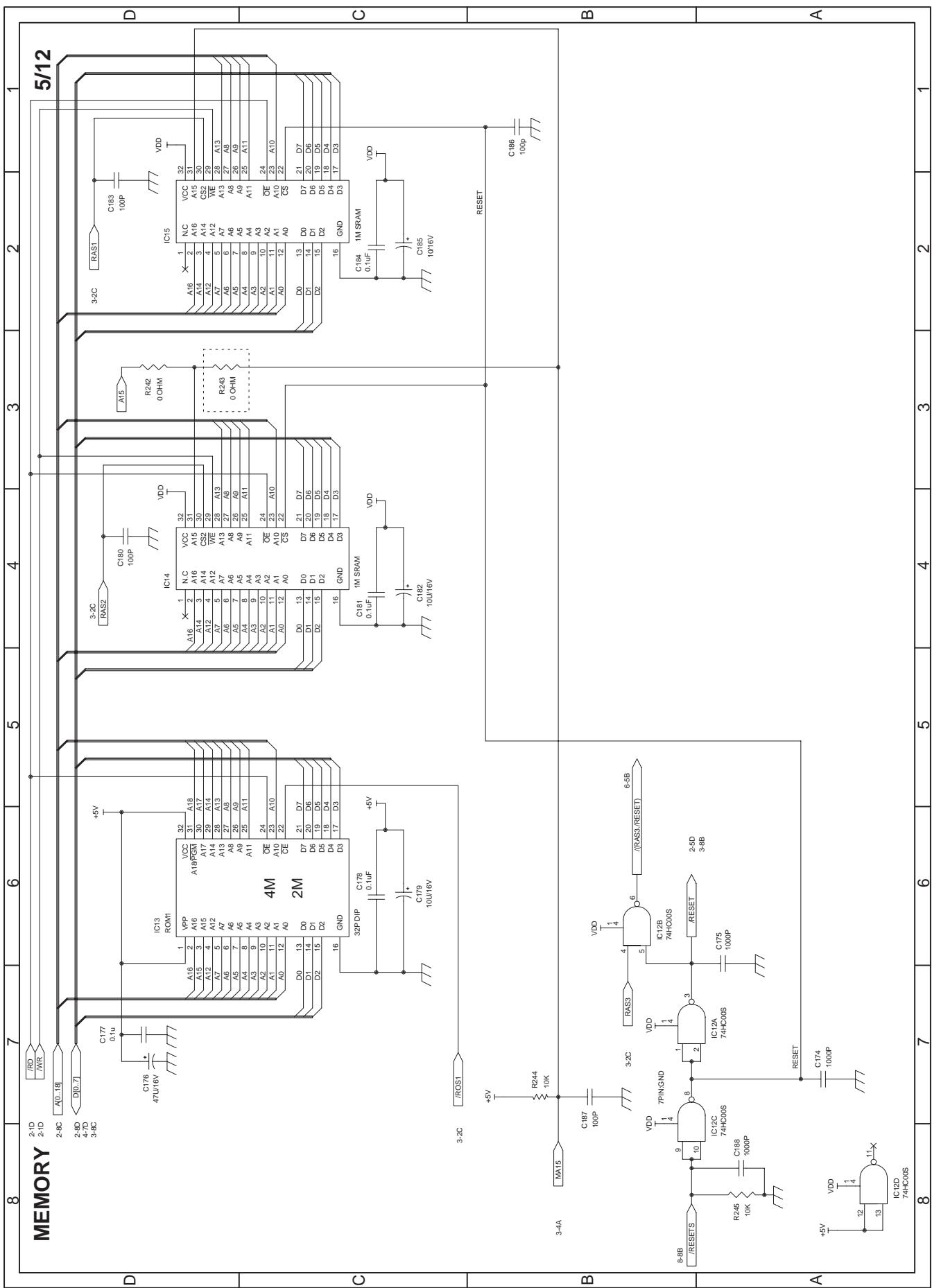
1/12



CPU(HD6415108)**2/12**

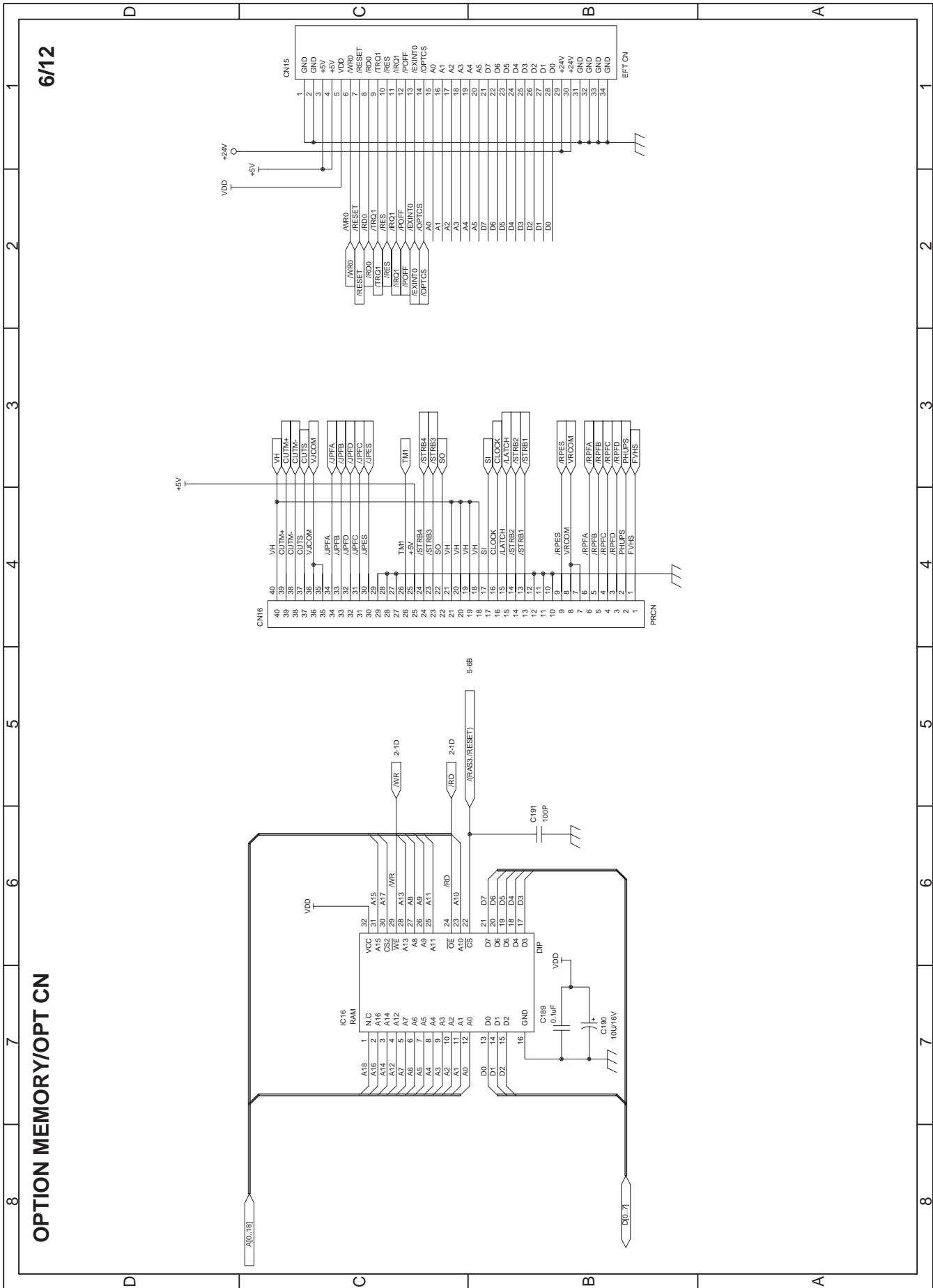


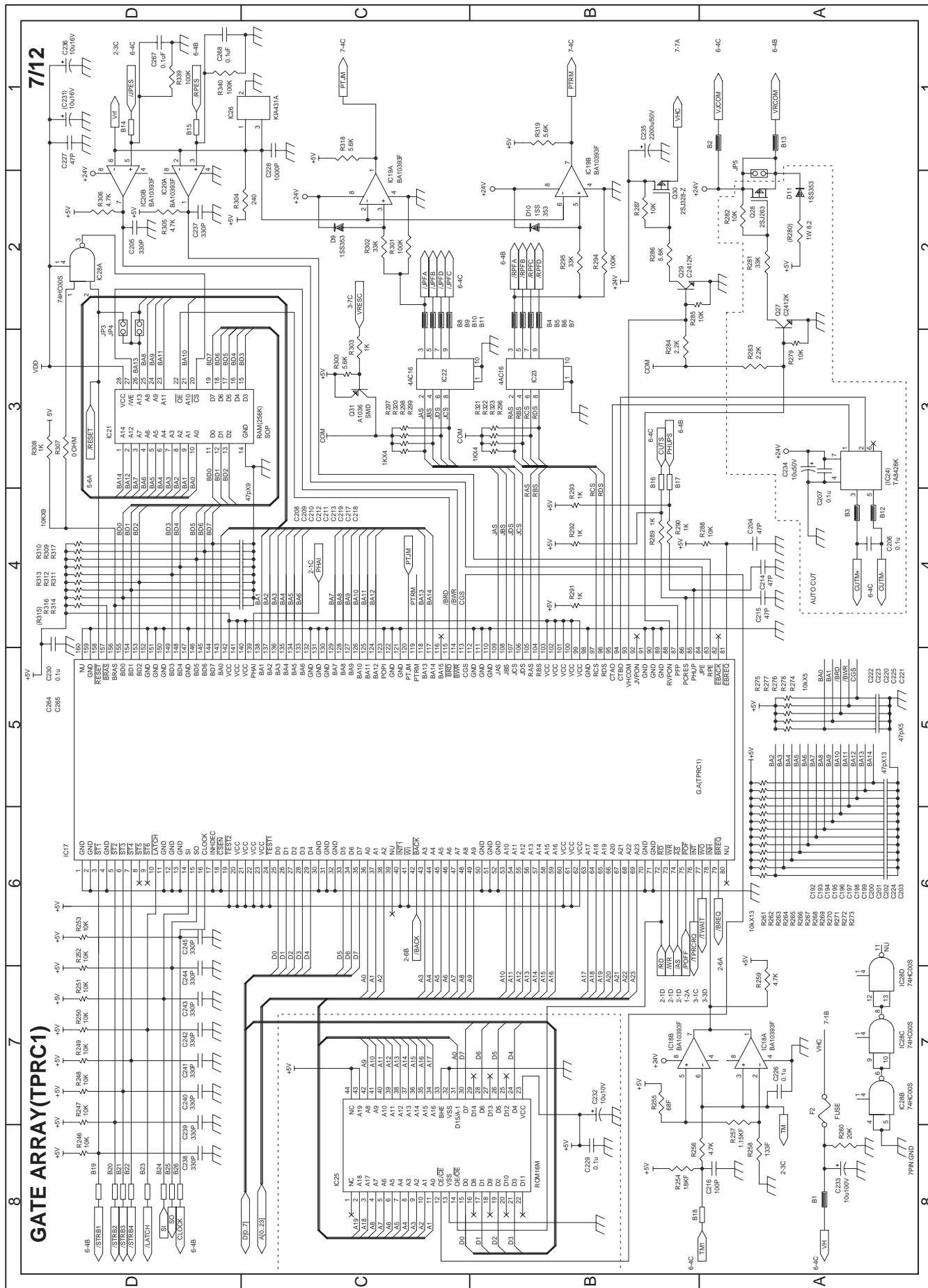
FMC (NOT USED)**4/12**



OPTION MEMORY/OPT CN

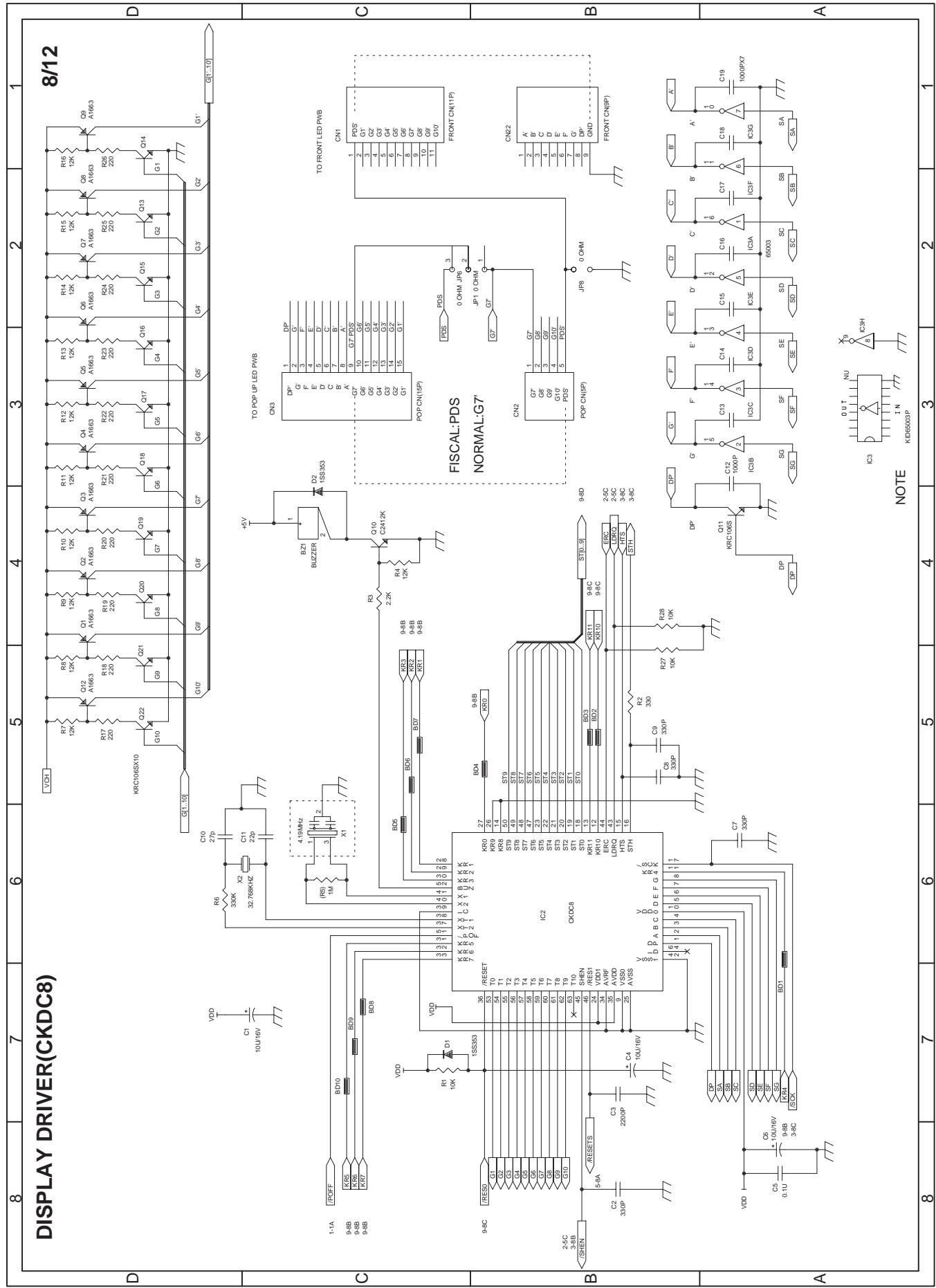
6/12





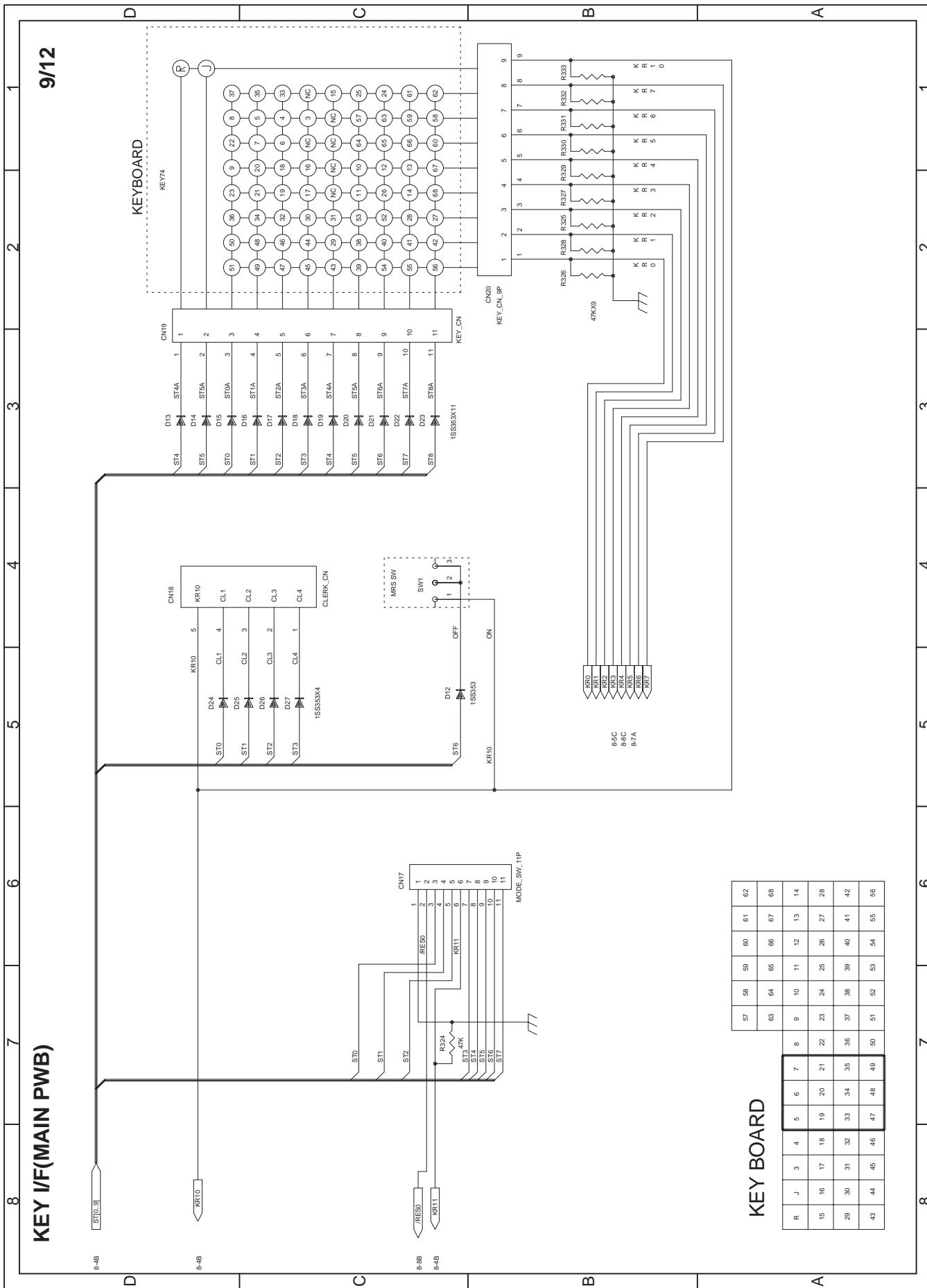
DISPLAY DRIVER(CKCDC8)

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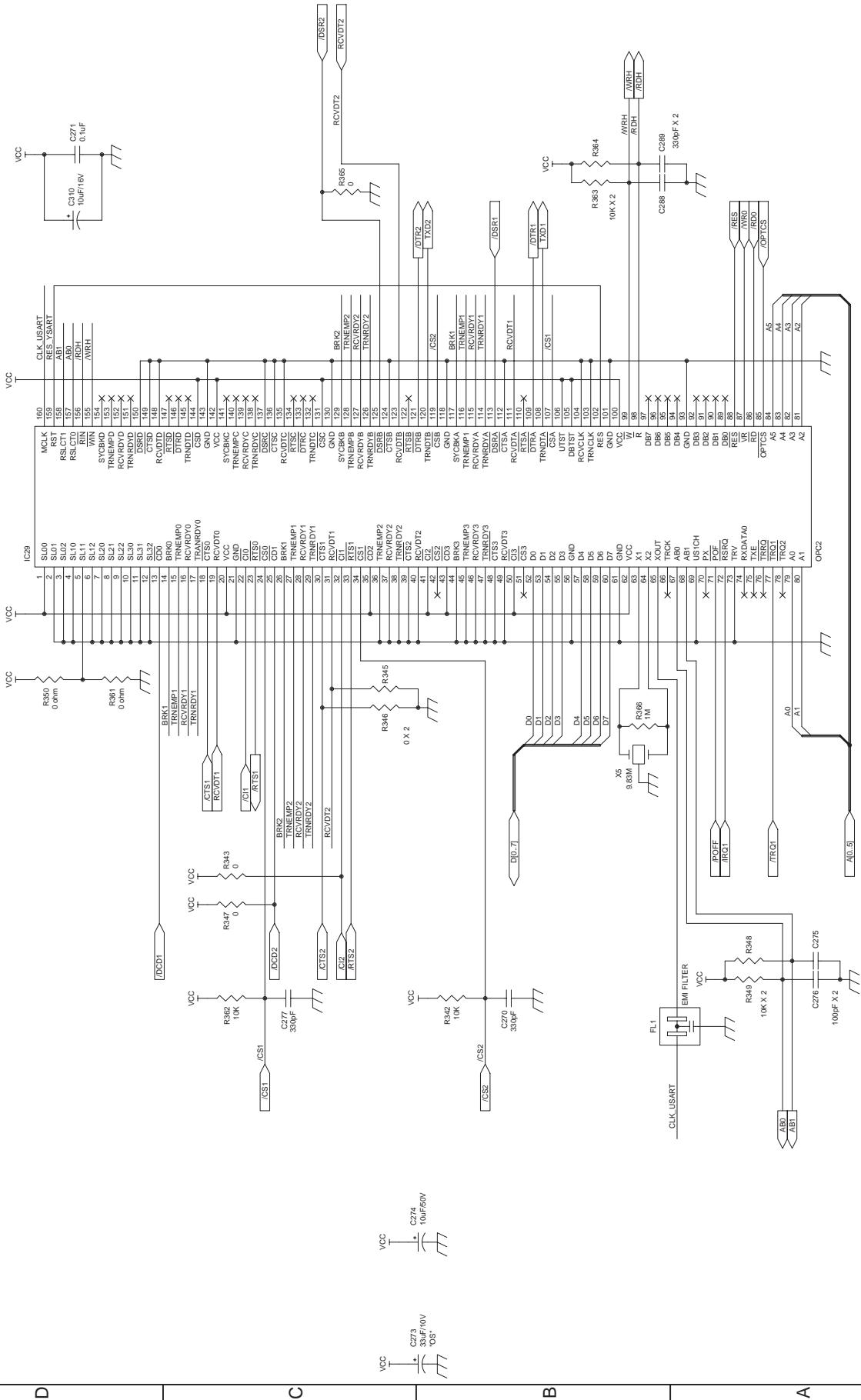
9/12

KEY I/F(MAIN PWB)



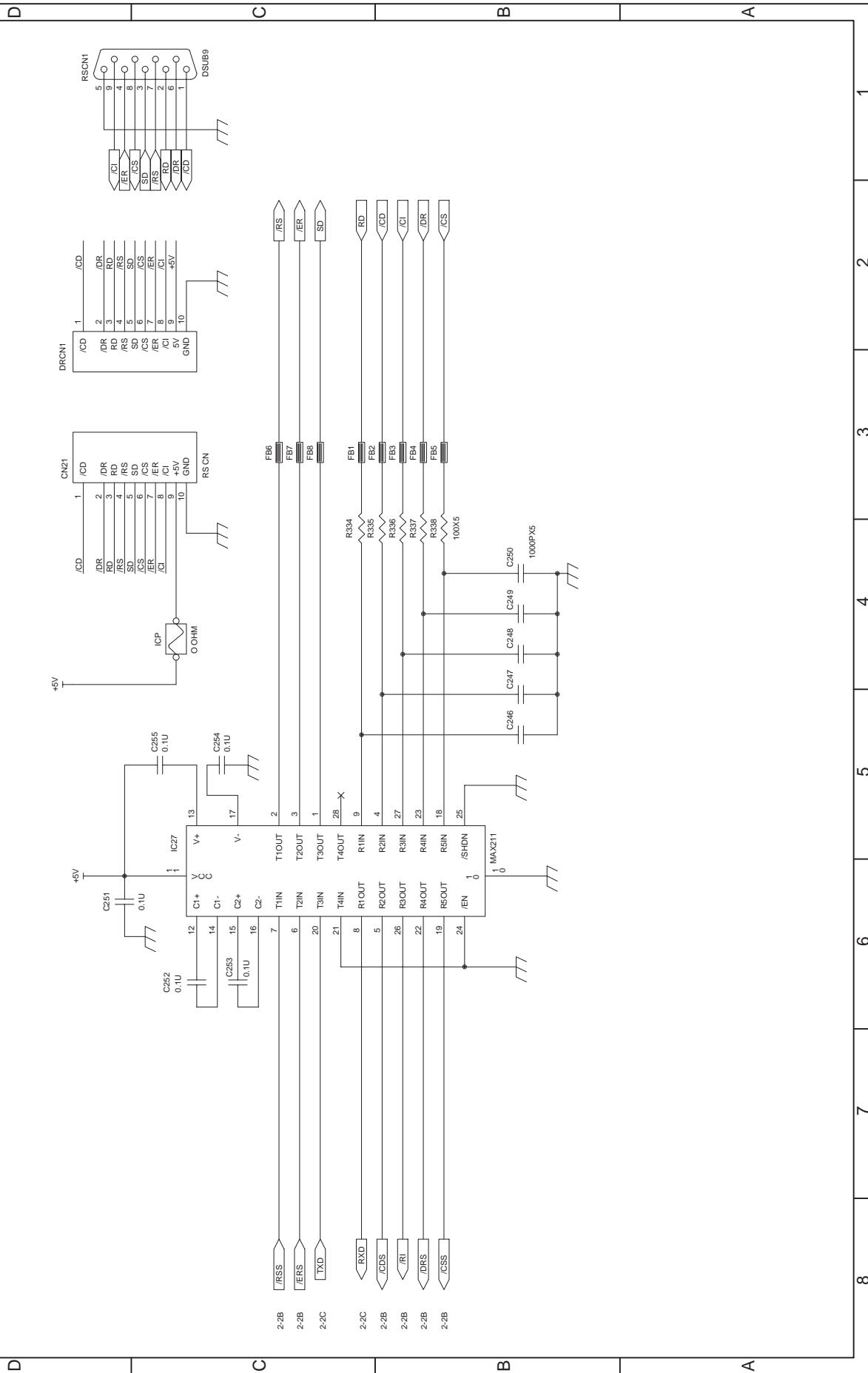
10/12

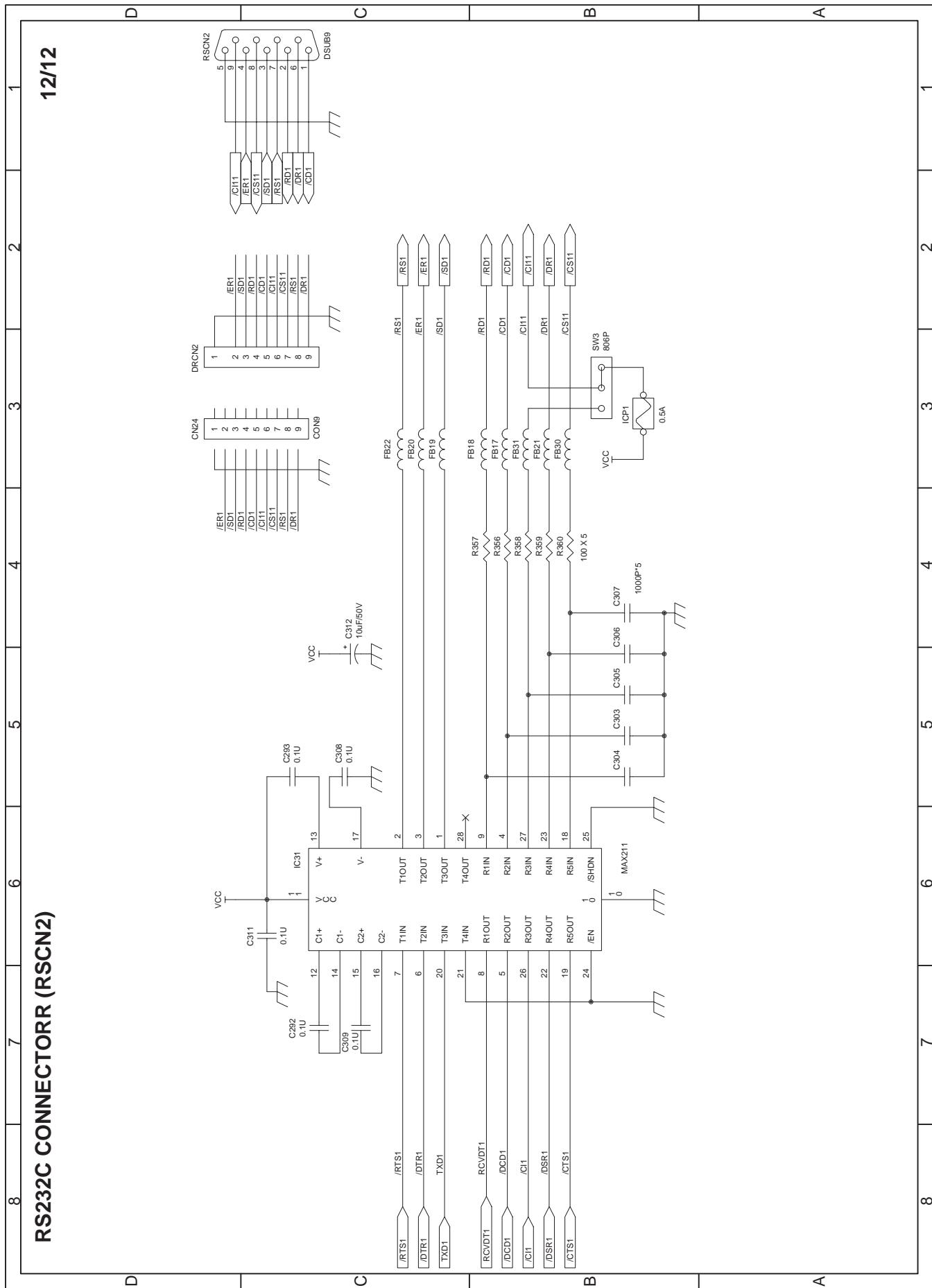
RS232C CIRCUIT DIAGRAM (OPC2)



RS232C CONNECTOR (RSCN1)

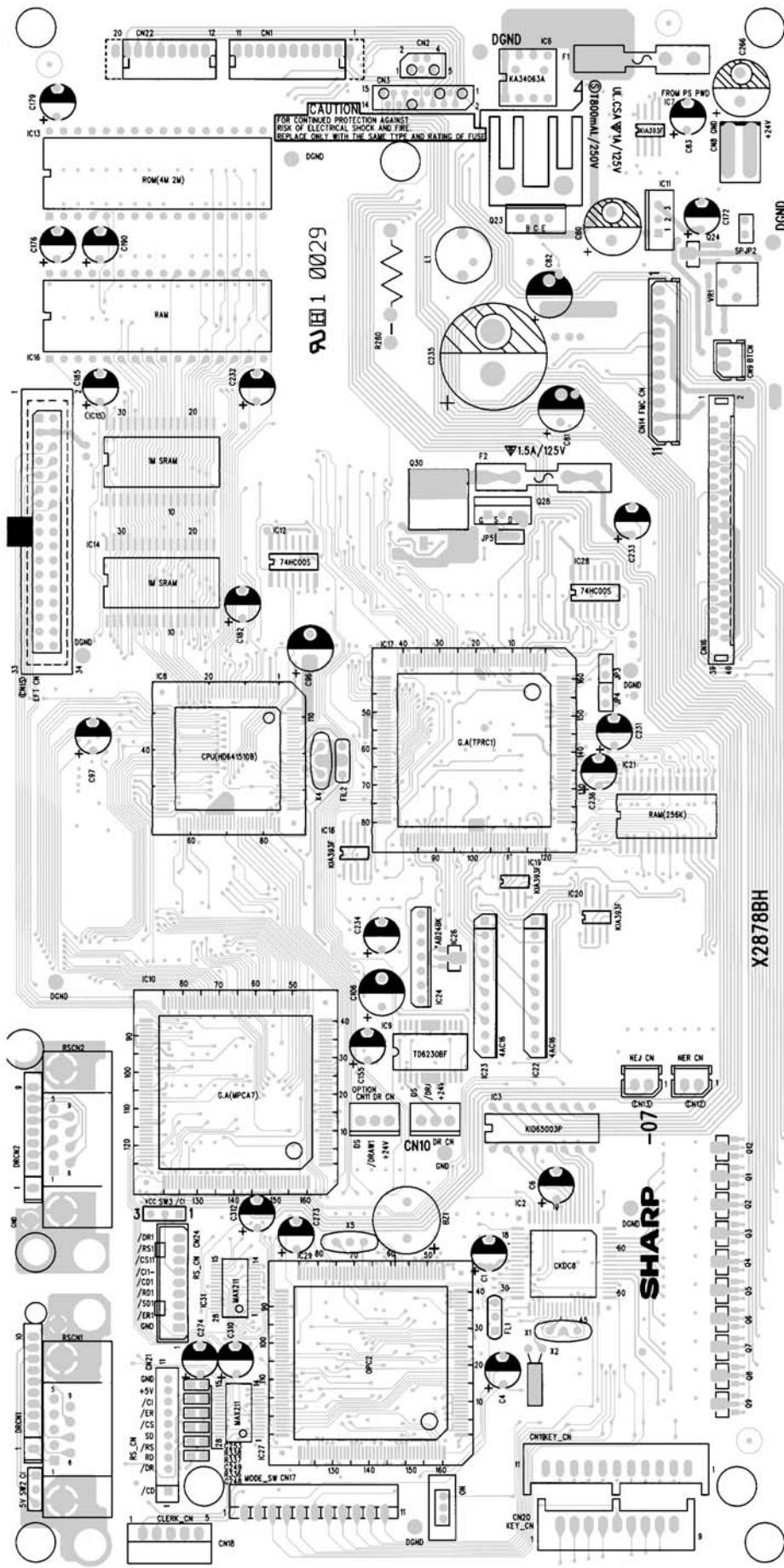
11/12

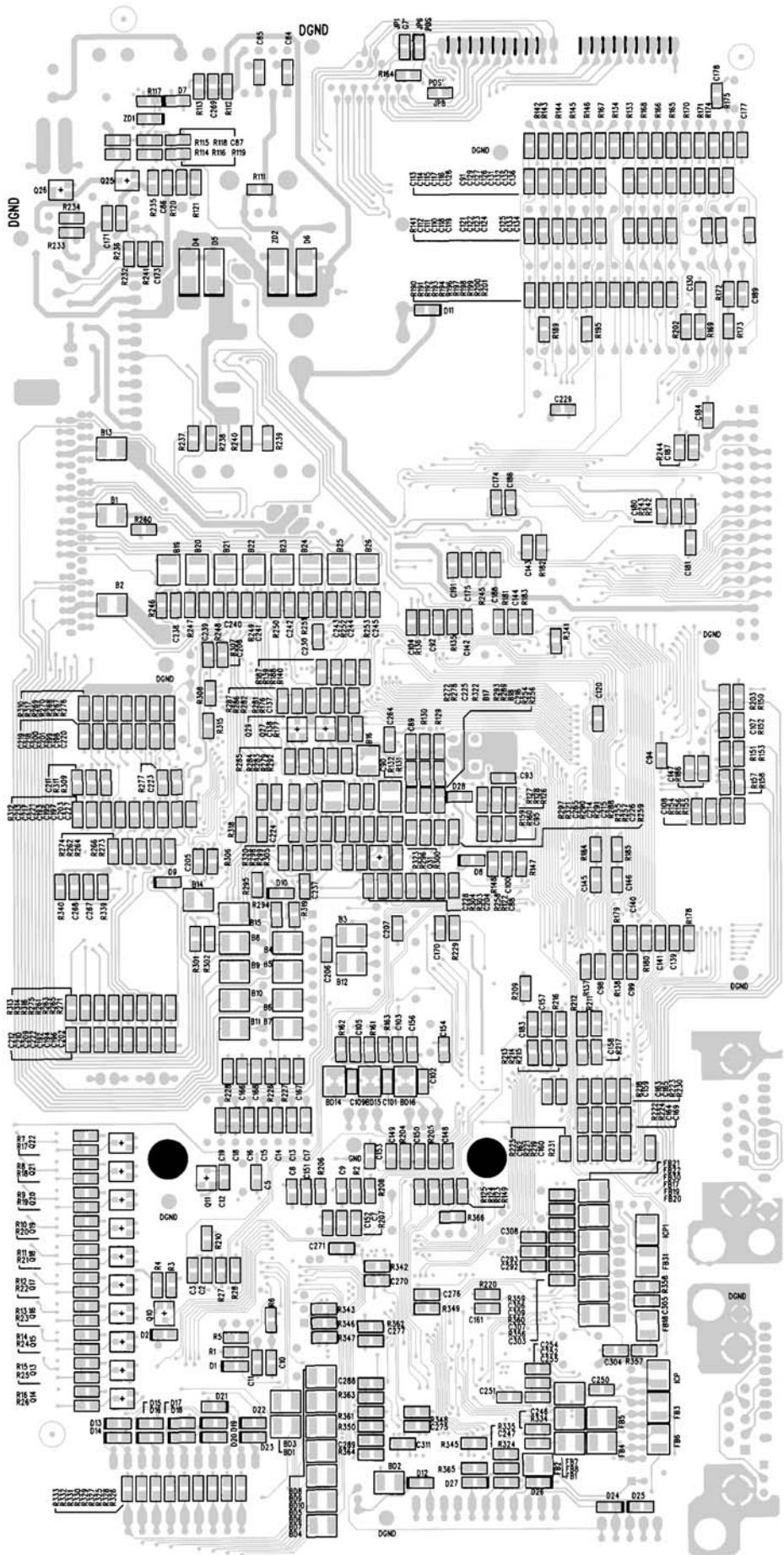


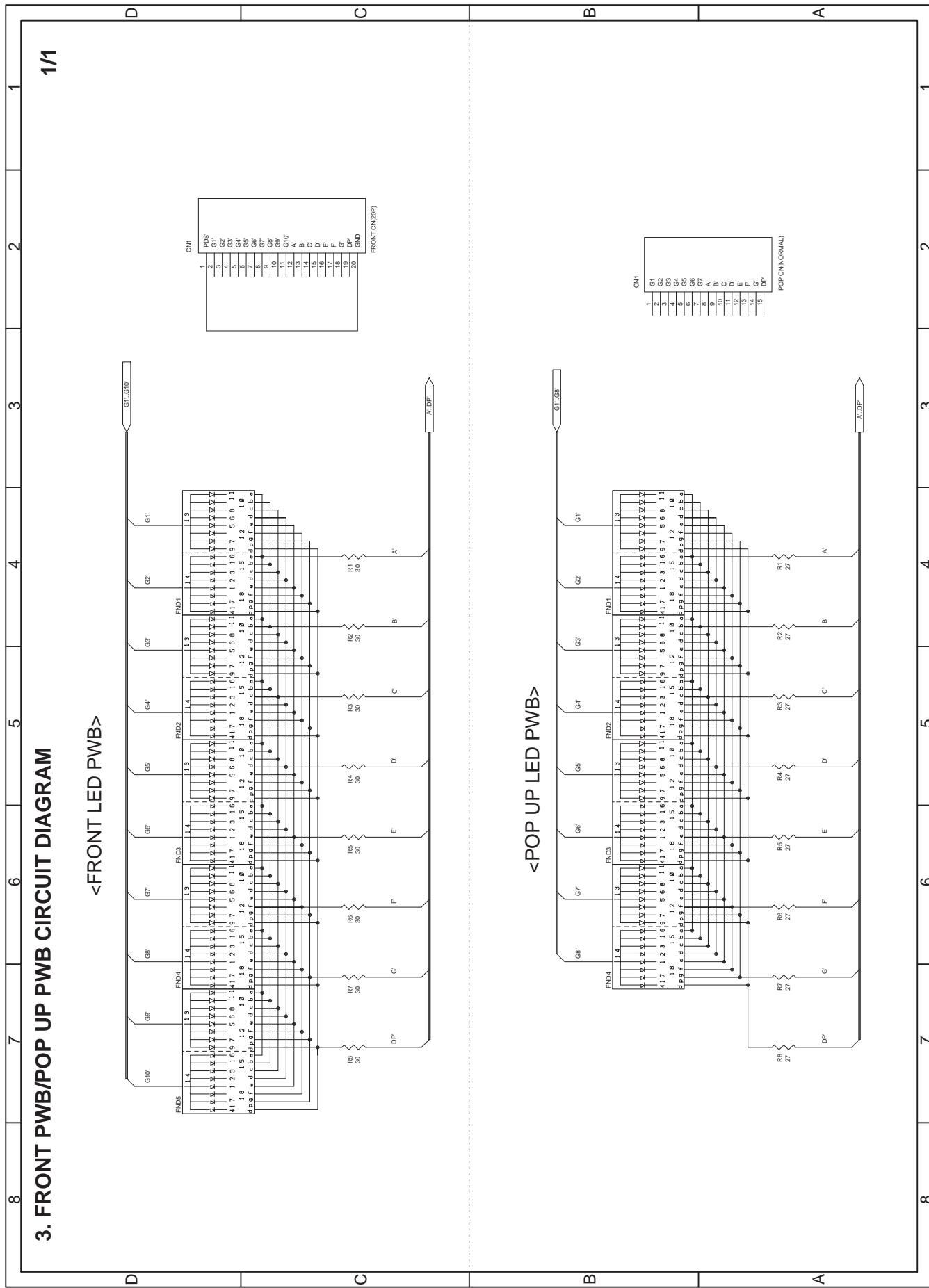


2. MAIN PWB LAYOUT

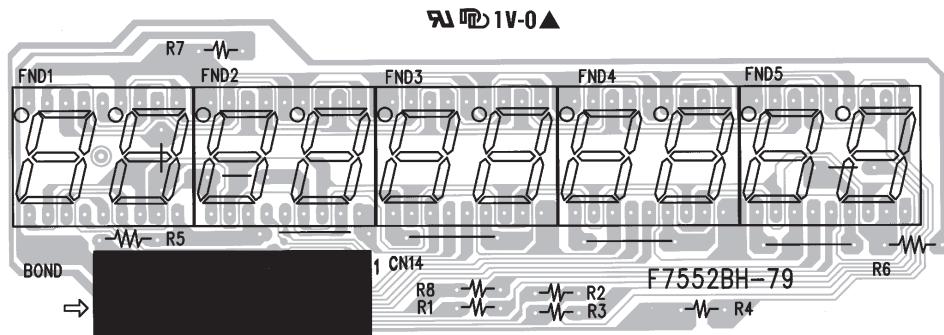
(1) SIDE A



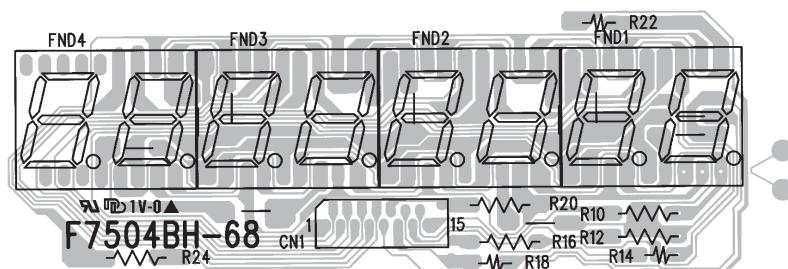




4. FRONT DISPLAY PWB LAYOUT

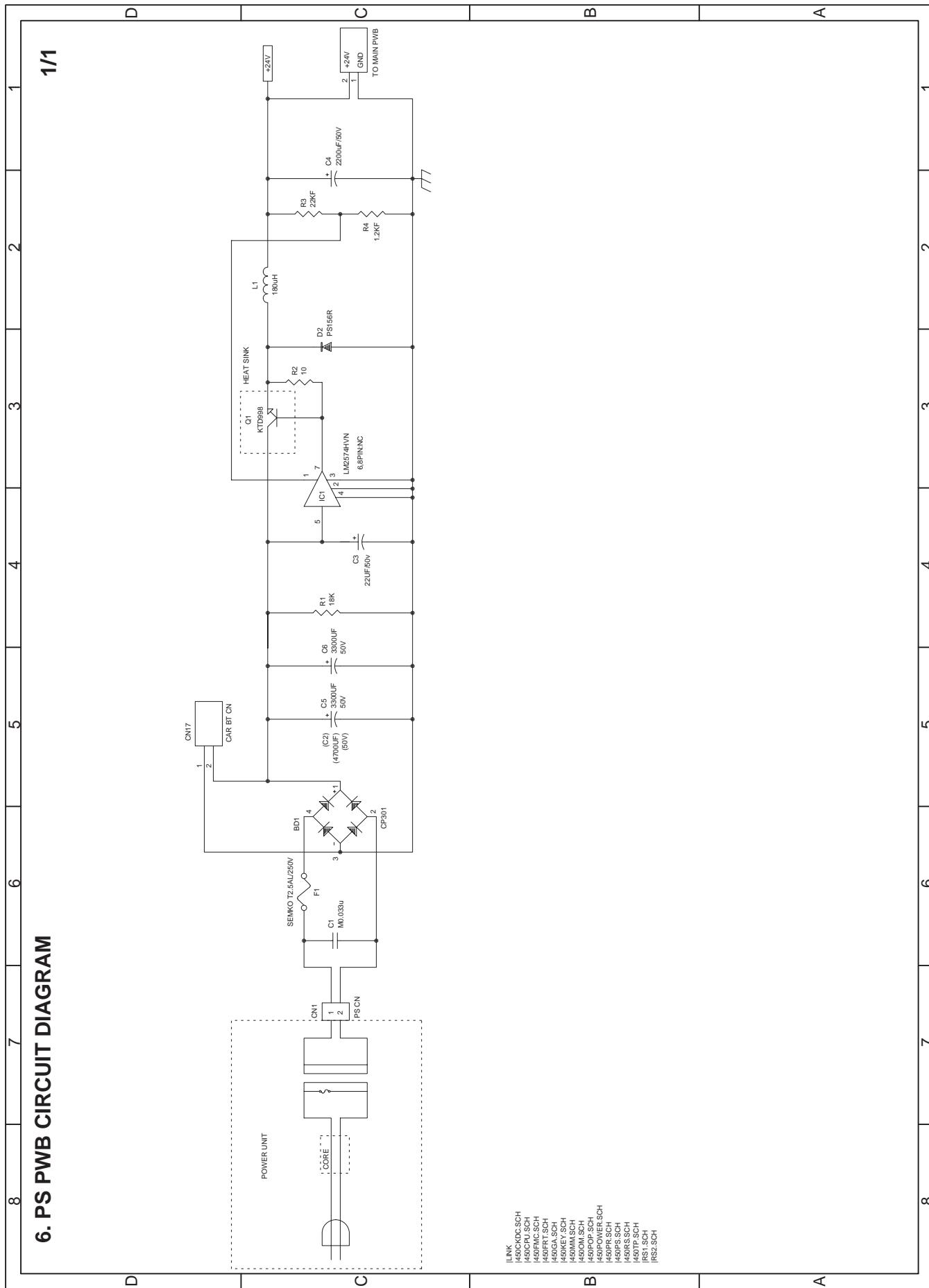


5. POP-UP DISPLAY PWB LAYOUT

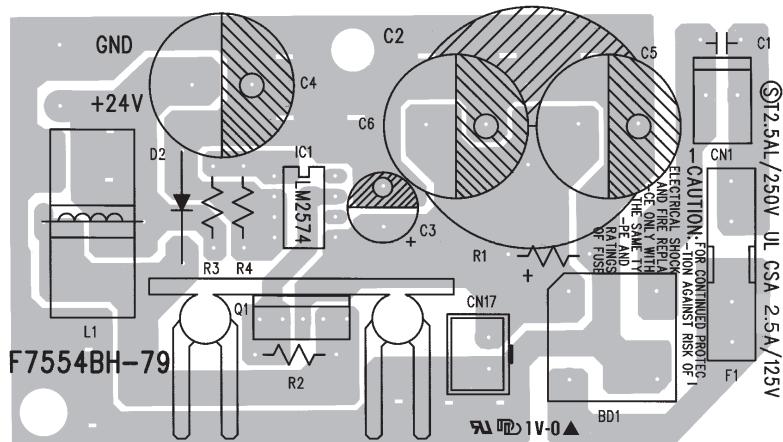


1/1

6. PS PWB CIRCUIT DIAGRAM



7. PS PWB LAYOUT



SHARP PARTS GUIDE

MODEL ER-A450S

**PRINTER:PR-45M
SRV key :LKGIM7113BHZZ**

(for TQ,TS,KA,KB)

CONTENTS

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| [1] Exterios | [8] Front LED PWB unit |
| [2] Keyboard unit | [9] Pop up LED PWB unit |
| [3] Packing material & Accessories | [10] Articles for consumption |
| [4] Drawer box unit(SK420 type) | [11] Service route options & Service tools |
| [5] Main PWB unit(include Block[6]) | ■ Index |
| [6] RS232C PWB unit | |
| [7] PS PWB unit | |

Because parts marked with "⚠" are indispensable for the machine safety maintenance and operation, it must be replaced with the parts specific to the product specification.

Table of destinations

SELECTION CODE	COUNTRIES
U	U.S.A., Guam
A	Canada
TS	Germany
TQ	SEEG territory other than Germany (Stamp:English)
TR	SEEG territory other than Germany (Stamp:English)
TM	SEEG(FRANCE:Metro-VM) (Stamp:French)
KB	U.Kingdom
KA	Australia

SELECTION CODE	COUNTRIES
K	Korea

SELECTION CODE	COUNTRIES
SB	Saudi Arabia (127V area)
SBA	Saudi Arabia (220V area)
SC	Taiwan
SD	Venezuela
SE	Hong Kong
SG	Lebanon, Syria, Greece, Pakistan, Iran, Egypt, Thailand, Iraq, Mauritius, Seychelles, Tahiti, Jordan, Sudan, Turkey
SH	South Africa (U.S.A. version)
SHE	South Africa (Europe version)
SJ	Philippines (Europe version)
SJ2	Philippines (U.S.A. version)
SM	Kuwait, Qatar, Oman, UAE, Malta, Bahrain
SMT	Nigeria, Yemen, Kenya

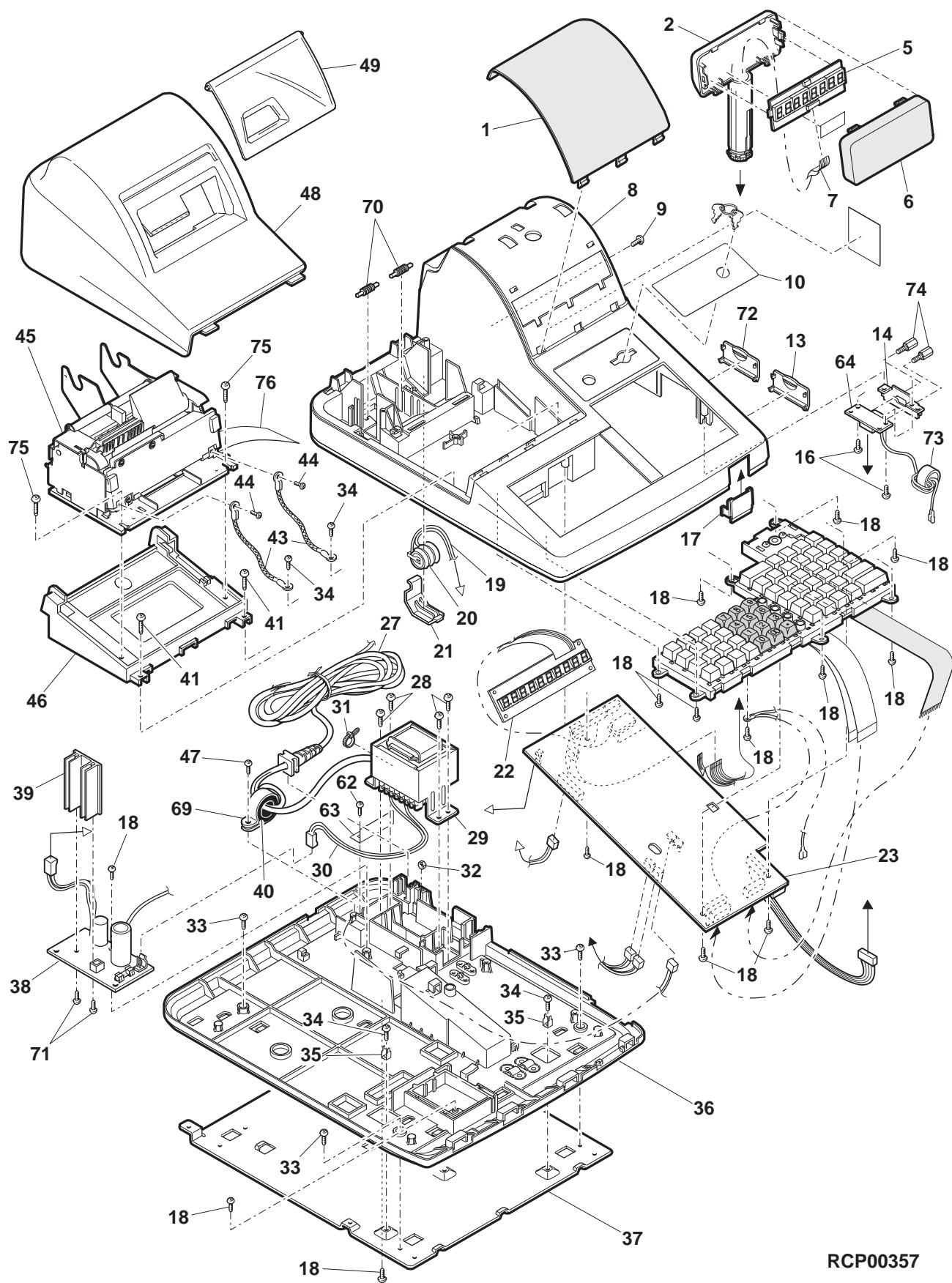
SELECTION CODE	COUNTRIES
RA1	Morocco, Algeria, Tunisia, West Africa
RA2	Chile, Uruguay, Peru, Argentina, Paraguay
RA5	Sri Lanka

SELECTION CODE	COUNTRIES
RB3	Indonesia
RB4	
RB5	Cyprus
RB6	Panama
RB7	Barbados
RB8	Malaysia (U.S.A. version)

SELECTION CODE	COUNTRIES
RC1	Malaysia (Europe version)
RC2	Singapore
RC5	Dominican Republic, Ecuador

1 Exteriors

1 Exteriors

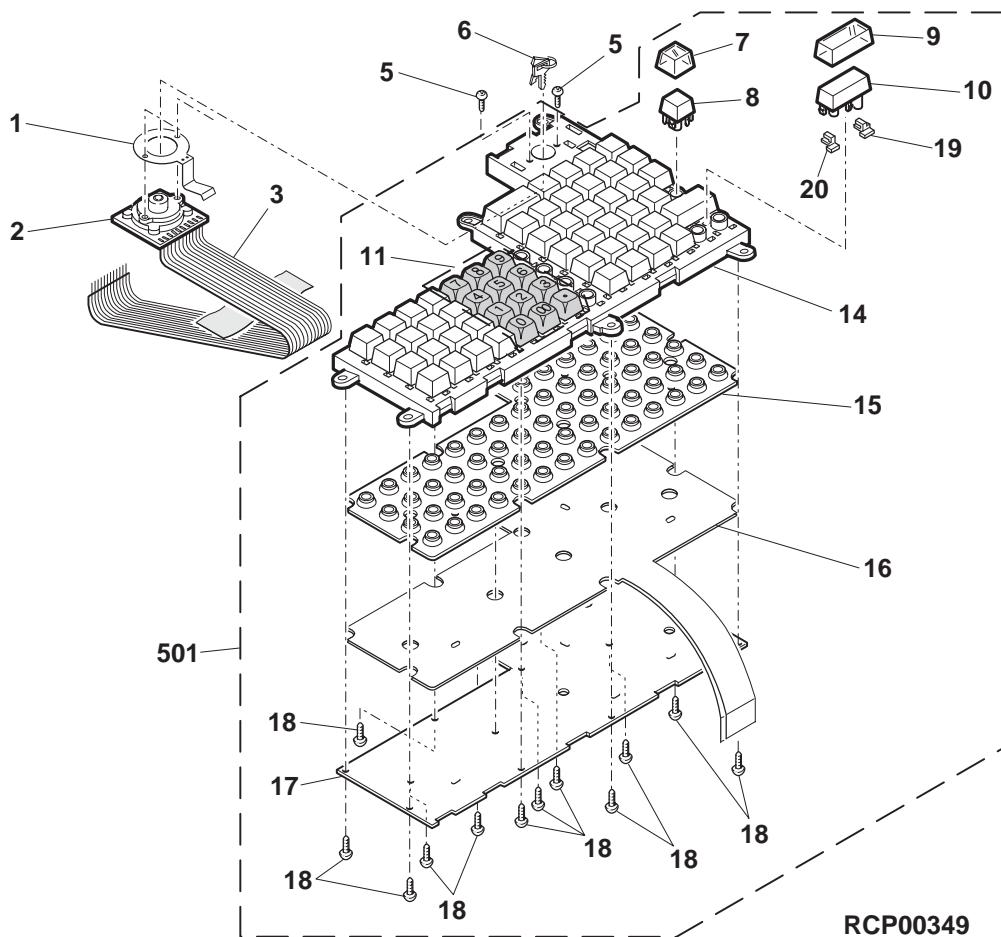


RCP00357

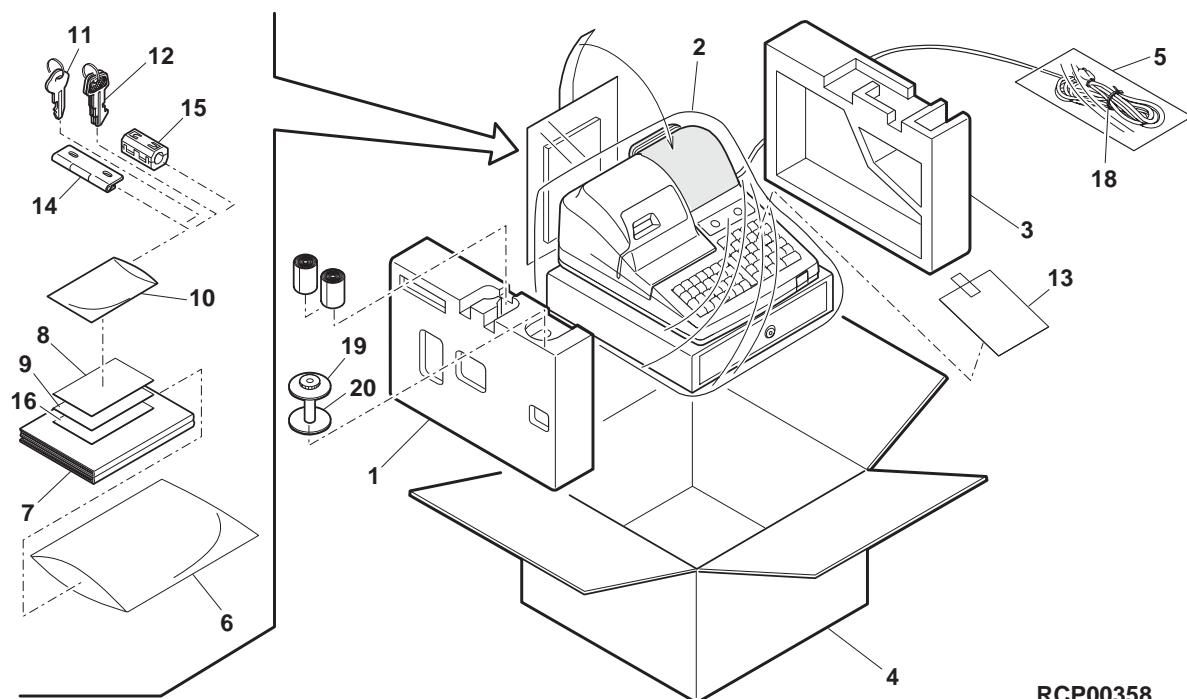
2 Keyboard unit

3 Packing material & Accessories

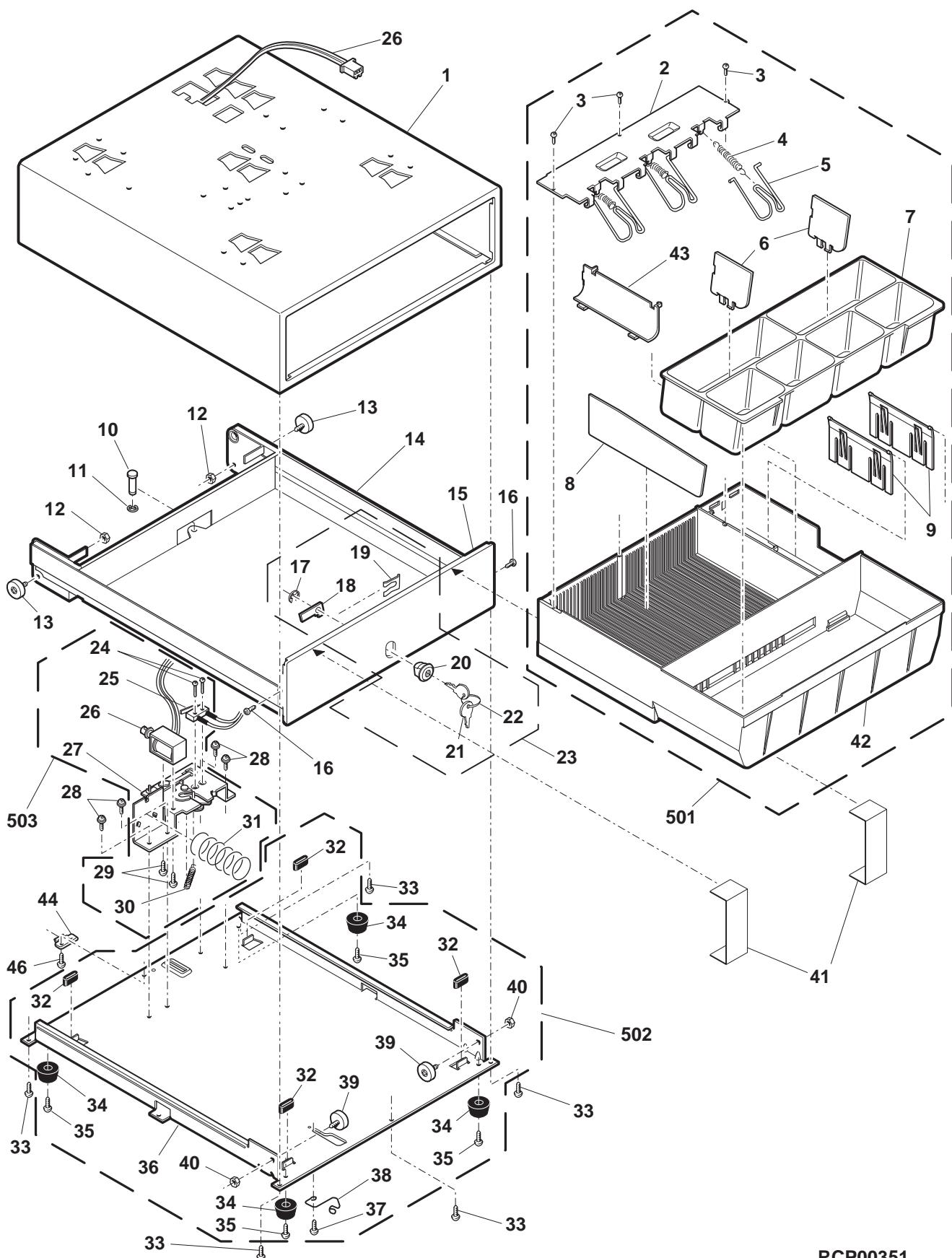
2 Keyboard unit



3 Packing material & Accessories



4 Drawer box unit(SK420 type)

4 Drawer box unit(SK420 type)

RCP00351

5 Main PWB unit(include Block[6])

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
1	PR D A F 6 6 5 6 B H Z Z	AK		C	Heat sink	[Q23]
2	QCNCM1101CCZZ	AB		C	Connector (2pin)(QCNCM1101BHZZ)	[CN8]
3	QCNCM7057RCZZ	AB		C	Connector (3pin)(QCNCM7057BHZZ)	[CN10,11]
4	QCNCM7207BH4J	AQ		C	Connector (Printer)(40P)(6229ZIF DIP)	[CN16]
5	QCNCW2423B0E	AE		C	Connector (Clerk)(5P)(5268-05A)	[CN18]
6	QCNCW6882BH1A	AG		C	Connector (11P)(52011-1110)(ST TYPE)	[CN17]
7	QCNCW7081BHZZ	AB		C	Connector (2P)(5267-02A)(Blue)	[CN9]
8	QCNCW7118BH0i	AG		C	Connector (K/B)(9P)(5229-09CPB)	[CN20]
9	QCNCW7118BH1A	AG		C	Connector (11P)(5229-11CPB)	[CN19]
10	QCNCW7201BH1E	AK		C	Connector (15P)(52806-1510)	[CN3]
11	QCNCW7245BH1J	AG		C	Connector (10P)(52007-1010)	[CN1]
12	QCNCW7246BH0H	AG		C	Connector (52007-0810)	[CN22]
13	QCNW-3098BHZZ	AP	N	C	DS CN cable 1	[CN21-DRCN1]
14	QCNW-3099BHZZ	AN	N	C	DS CN cable 2(RS232 cable)	[DRCN2]
15	QCNW-7889BHZZ	AG		C	GND wire (M.PWB ↔ K/B ↔ DRAWER)	[M.PWB-K/B,DRAWER]
16	QFS-A1037CCZZ	AC		A	Fuse (1.5A)(MINI TYPE)	[F2]
17	QFS-C4301CCZZ	AE		A	Fuse (T800mA/250V)(QFS-C4301BHZZ)	[F1]
18	QFSHD2109AFZZ	AC		C	Fuse holder (HD2109AF)	[F1,F2]
19	QSOCZ2042SC32	AE		C	IC socket (32pin)	[IC13,16]
20	RALMB6646RCZZ	AN		B	Buzzer (RALMB6646BHZZ)	[BZ1]
21	RC-EZ336ARC1A	AB		C	Capacitor (10WV 33μF)	[C273]
22	RCILC6647RCZZ	AE		C	Coil (220μH)(RCH-110)(RCILC6647BHZZ)	[L1]
23	RCORF6702BHZZ	AF		C	EMI filter (100pF)	[FL1,FL2]
24	RCORF7002BHZZ	AE		C	Chip core (EFCB322513TS)	[B1,2,4,5,6,7,8,9,10,11,13]
	RCORF7002BHZZ	AE		C	Chip core (EFCB322513TS)	[B14,15,16,17,18,19,20,21,22,23,24,25,26]
	RCORF7002BHZZ	AE		C	Chip core (EFCB322513TS)	[BD1,2,3,4,5,6,7,8,9,10,]
	RCORF7002BHZZ	AE		C	Chip core (EFCB322513TS)	[FB1,2,3,4]
	RCORF7002BHZZ	AE		C	Chip core (EFCB322513TS)	[FB5,6,7,8]
	RCORF7002BHZZ	AE		C	Chip core (EFCB322513TS)	[FB17,18,19,20,21,22,30,31]
25	RCRSP6664RCZZ	AF		B	Crystal (19.66MHz)	[X4]
26	RCRSP6676RCZZ	AG		B	X-TAL (32.768KHz)	[X2]
27	RCRSZ6644RCZZ	AD		B	Crystal (4.19MHz)	[X1]
28	RCRSZ6662RCZZ	AE		B	Crystal (9.83MHz)	[X5]
29	VCCCTV1HH101J	AA		C	Capacitor (50WV 100PF)	[C88,90,91,92,104,110,111,112,113,114,115]
	VCCCTV1HH101J	AA		C	Capacitor (50WV 100PF)	[C116,117,118,119,120,121,122,123,124,125]
	VCCCTV1HH101J	AA		C	Capacitor (50WV 100PF)	[C126,127,128,129,130,131,132,133,134,135]
	VCCCTV1HH101J	AA		C	Capacitor (50WV 100PF)	[C136,137,138,139,140,141,170,180,183,186]
	VCCCTV1HH101J	AA		C	Capacitor (50WV 100PF)	[C187,191,216,275,276]
30	VCCCTV1HH220J	AA		C	Capacitor (50WV 22PF)	[C11]
31	VCCCTV1HH221J	AA		C	Capacitor (50WV 220PF)	[C85]
32	VCCCTV1HH270J	AC		C	Capacitor (50WV 27pF)	[C10]
33	VCCCTV1HH331J	AA		C	Capacitor (50WV 330PF)	[C2,7,8,9,98,99,145,146,147,149,150,151,]
	VCCCTV1HH331J	AA		C	Capacitor (50WV 330PF)	[C152,153,157,158,159,160,161,162,163,]
	VCCCTV1HH331J	AA		C	Capacitor (50WV 330PF)	[C164,165,169,205,237,238,239,240,241,]
	VCCCTV1HH331J	AA		C	Capacitor (50WV 330PF)	[C242,243,244,245,270,277,288,289]
34	VCCCTV1HH470J	AA		C	Capacitor (50WV 47PF)	[C89,192,193,194,195,196,197,198,199,200]
	VCCCTV1HH470J	AA		C	Capacitor (50WV 47PF)	[C201,202,203,204,208,209,210,211,212,213]
	VCCCTV1HH470J	AA		C	Capacitor (50WV 47PF)	[C214,215,217,218,219,220,221,222,223,224]
	VCCCTV1HH470J	AA		C	Capacitor (50WV 47PF)	[C225,227]
35	VCEAGA1CW106M	AA		C	Capacitor (16WV 10μF)	[C1,4,6,179,182,185,190,236]
36	VCEAGA1CW106M	AA		C	Capacitor (16WV 10μF)	[C274,310,312]
37	VCEAGA1CW337M	AB		C	Capacitor (16WV 330μF)	[C81,82]
38	VCEAGA1CW476M	AB		C	Capacitor (16WV 47μF)	[C96,97,176]
39	VCEAGA1HW106M	AA		C	Capacitor (50WV 1μF)	[C83]
40	VCEAGA1HW107M	AA		C	Capacitor (50WV 10μF)	[C155]
41	VCEAGA1HW228M	AB		C	Capacitor (50WV 2200μF)	[C235]
42	VCEAGD1CW108M	AE		C	Capacitor (16WV 1000μF)	[C80]
43	VCEAGU2AW106M	AB		C	Capacitor (100WV 10μF)	[C233]
44	VCKYTV1HB102K	AA		C	Capacitor (50WV 1000PF)	[C12,13,14,15,16,17,18,19,87,105,107,]
	VCKYTV1HB102K	AA		C	Capacitor (50WV 1000PF)	[C108,142,143,144,166,167,168,174,188,228]
	VCKYTV1HB102K	AA		C	Capacitor (50WV 1000PF)	[C246,247,250,303,304,305,306,307]
	VCKYTV1HB102K	AA		C	Capacitor (50WV 1000PF)	[C248,249]
45	VCKYTV1HB103K	AB		C	Capacitor (50WV 0.010μF)	[C148]
46	VCKYTV1HB222K	AA		C	Capacitor (50WV 2200pF)	[C3]
47	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10μF)	[C5,84,86,93,94,95,101,102,103,109,154,156]
	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10μF)	[C177,178,181,184,189]
	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10μF)	[C226,230,251,252,254]
	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10μF)	[C253]
48	VHD1SR1544001	AB		B	Diode (1SR1544001)	[D4,5]
49	VHD1SS353// - 1	AB		B	Diode (1SS353)	[D1,2,8,13,14,15,16,17,]
50	VHD1SS353// - 1	AB		B	Diode (1SS353)	[D18,19,20,21,22,23,24,25,26,27,28]
51	VHEPTZ6 . 2 A / - 1	AH		B	Zener diode (PTZ6.2A)	[ZD2]
52	VHEUDZ5 . 1 B / - 1	AC		B	Zener diode (UDZ5.1B)	[ZD1]
53	VH i 27040RBV1A	BN	N	B	EPROM (4M T27C04010)(27040RBV1A)	
54	VH i 4 AC16 // / - 1	AK		B	IC (4AC16)	[IC22,23]
55	VH i 5108CP7H - 1	AW		B	S-RAM (1M SOP)(5108CP7H-1)	[IC14,IC15]
56	VH i BA10393F - 1	AC		B	IC (BA10393F)	[IC7,18,20]

5 Main PWB unit(include Block⑥)

6 RS232C PWB

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	QCNCM1060AC03	AB		C	Connector (Short Pin 3P) [SW2,SW3]
2	QCNCM7125BH0i	AN		C	Connector ((9P) MLX 87023-6066)) [RS CN1,RSCN2]
3	QCNCM7176BH0i	AD		C	Connector (Key)(53014-0910) [CN24(MALE_TYPE)]
4	QCNCW1057ACZZ	AB		C	Connector (Short socket) [SW2-CI,SW3-1]
5	QCNW-7890BHZZ	AF		C	GND wire (RS.PWBDRAWER) [DRCN1,DRCN2]

7 PS PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	LX-BZ6644BHZZ	AA		C	Screw (M3.5x8S) [Q1(HEAT SINK fixed)]
2	PRDAF6666BHZA	AN		C	Heat sink [Q1]
3	QCNCM1101BHZZ	AC		C	Connector (5273-2)(2P) [CN1]
4	QCNCW7242BH0B	AD		C	Connector (35313-0210) [CN17]
5	QCNW-7915BHZZ	AL		C	PS DC cable [+24V , GND]
6	QCNW-7886BHZZ	AG		C	GND wire [PWB-TRANS]
7	QFS-C2521TAZZ	AE		A	Fuse (T2.5AL/250V) [F1]
8	QFSHD2109AFZZ	AC		C	Fuse holder (HD2109AF) [F1]
9	RCiLC6653BHZZ	AS		C	Choke coil (180μH) [L1]
10	VCEAGA1HW226M	AB		C	Capacitor (50WV 22μF) [C3]
11	VCEAGA1HW228M	AB		C	Capacitor (50WV 2200μF) [C4]
12	VCEAGU1HW338M	AT		C	Capacitor (50WV 3300μF)(VCEAGA1HW338M) [C5,6]
13	VCQYNA1HM333K	AA		C	Capacitor (50WV 0.033μF) [C1]
14	VHDCP301///-1	AL		B	Diode (CP301) [BD1]
15	VHDPS156///-1	AE		B	Diode (PS156R) [D2]
16	VHiLM2574HVN-ADJ	AU		B	IC (LM2574HVN-ADJ) [IC1]
17	VRD-RC2EY100J	AA		C	Resistor (1/4W 10Ω ±5%) [R2]
18	VRD-RC2EY122G	AA		C	Resistor (1/4W 1.2KΩ ±2%)(VRD-RC2EY122F) [R4]
19	VRD-RC2EY183J	AA		C	Resistor (1/4W 18KΩ ±5%) [R1]
20	VRD-RC2EY223G	AA		C	Resistor (1/4W 22KΩ ±2%)(VRD-RC2EY223F) [R3]
21	VSKTD998///-1	AS		B	Transistor (2SD998) [Q1]
22	XBSD30P06000	AA		C	Screw (M3×6) [Q1(TR fixed)]
	(Unit)				
901	CPWBF7554BH03	BP		E	PS PWB unit

8 Front LED PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	QCNW-7877BHZZ	AN		C	Front LED cable (18P) [BOND]
2	VPHDSP5621-1	AM		B	LED (2SEG GREEN)(HDSP5621) [FND1,2,3,4,5]
3	VRD-RC2EY300J	AA		C	Resistor (1/4W 30Ω ±5%) [R1,2,3,4,5,6,7,8]
	(Unit)				
901	CPWBF7552BH01	BC		E	Front LED PWB unit

9 Pop up LED PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	QCNCW7202BH1E	AK		C	Connector (52807-1510) [CN1]
2	QCNW-7878BHZZ	AK		C	Flat cable (15P) [CN1]
3	VPHDSP5621-1	AM		B	LED (2SEG GREEN)(HDSP5621) [FND1-FND4]
4	VRD-RC2EY270J	AA		C	Resistor (1/4W 27Ω ±5%) [R10,12,14,16,18,20,22,24]
	(Unit)				
901	CPWBF7504BH01	BC		E	Pop up LED PWB unit (NORMAL)

10 Articles for consumption

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	T P A P R 6 4 5 R C 0 5	AY		S	Roll paper (5rolls/pack)

11 Service route options & Service tools

■ Index

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK	
[C]					
CCABM7863BHZZ	4- 1	BF		D	
CCASP6700BH08	4-501	BK		E	
CDRW-6681BH02	4- 14	BE		D	
CDRW-6683BHZZ	4-504	BL		D	
CFRM-6701BH01	4- 27	AY		D	
CLABH7092BH01	2-101	AN	N	D	
CPLTM6708BH01	4-502	BF		E	
CPLU-6647BH01	4- 26	AY		B	
CPWBF7504BH01	1- 5	BC		E	
"	9-901	BC		E	
CPWBF7552BH01	1- 22	BC		E	
"	8-901	BC		E	
CPWBF7554BH03	1- 38	BP		E	
"	7-901	BP		E	
CPWBX2878BH01	1- 23	CL	N	E	
"	1- 64	CL	N	E	
"	5-901	CL	N	E	
[D]					
DKiT-8669BHZZ	11- 6			S	
DUNT-1306BHZA	4- 23	AX		E	
DUNTK0247BH01	2-501	BN	N	E	
DUNTK3677BH03	11- 4	BB		S	
DUNTM5818BHZZ	4-503	BE		E	
[G]					
GBOXD7153BHZZ	4-901	BY		E	
GCABA7858BHZG	1- 36	BB	N	D	
GCABB7857BHZE	1- 8	BD	N	D	
GCABB7861BHZZ	1- 2	AN		D	
GCASP6700BHZC	4- 42	BC		D	
GCASP6701BHZZ	4- 7	AV		D	
GCÖVA7140BHZZ	1- 48	AZ		D	
GCÖVA7147BHZZ	4- 15	AS		D	
GCÖVB7153BHZZ	11- 5	BH		S	
GCOVH2509BHZZ	1- 72	AG		D	
GCÖVH7126BHZZ	11- 3	BE		S	
GCOVH7143BHZZ	1- 21	AH		D	
GCOVH7144BHZZ	1- 13	AH		D	
GCÖVH7147BHZZ	1- 63	AK		D	
GFTAF6921BHSC	1- 17	AH		D	
[H]					
HDECP6864BHSA	1- 10	AM	N	D	
[J]					
JKNBZ6896BHZA	2- 8	AG		C	
JKNBZ6897BHSA	2- 7	AH		C	
JKNBZ6898BHZZ	2- 10	AH		C	
JKNBZ6899BHSA	2- 9	AK		C	
JKNBZ6902BHSB	11- 7	AH		S	
JKNBZ6903BHSB	11- 8	AR		S	
JKNBZ6905BHZZ	2- 11	AF		C	
JKNBZ6908BHZZ	2- 11	AK		C	
JKNBZ6911BHZZ	2- 11	AK		C	
JKNBZ6912BHZZ	2- 11	AK		C	
JKNBZ6913BHZZ	2- 11	AK		C	
JKNBZ6914BHZZ	2- 11	AK		C	
JKNBZ6915BHZZ	2- 11	AK		C	
JKNBZ6916BHZZ	2- 11	AK		C	
JKNBZ6917BHZZ	2- 11	AK		C	
JKNBZ6918BHZZ	2- 11	AK		C	
JKNBZ6919BHZZ	2- 11	AK		C	
JKNBZ6920BHZZ	2- 11	AK		C	
[K]					
KiT-OB2359BHZZ	1- 45	CA		E	
[L]					
LANGK2897BHZZ	1- 14	AQ	N	C	
LANGK7612BHZZ	4- 44	AF		C	
LANGK7613BHZZ	3- 14	AN		C	
LANGQ7604BHZZ	2- 1	AG		C	
LBNDJ2003SCZZ	1- 31	AA		C	
LBNDJ6636BHZZ	1- 69	AD		C	
LCHSM6706BHZZ	1- 37	BA		C	
LFRM-6700BHZZ	2- 14	BB		D	
LHLDZ6836BHZZ	2- 19	AE		C	
LHLDZ6837BHZZ	2- 20	AE		C	
LHLDZ6847BHZZ	1- 46	AS		C	
LKGiTM1004BH01	11-101	AW		S	
LKGiTM1004BH02	11-102	AW		S	
LKGiTM1004BH03	11-103	AW		S	
LKGiTM1004BH04	11-104	AW		S	

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK	
LKGiTM1004BH05	11-105	AW		S	
LKGiTM1004BH06	11-106	AW		S	
LKGiTM7110BHZZ	2- 6	AE		B	
"	3- 12	AE		B	
LKGiTM7111BHZZ	2- 6	AE		B	
"	3- 12	AE		B	
LKGiTM7113BHZZ	11- 1	AF		S	
LKGiTM7126RCZZ	11- 2	AL		S	
LKGiTM7129BHZZ	2- 6	AE		B	
"	3- 12	AE		B	
LKGiTM7331BHZZ	3- 11	AE		B	
"	4- 21	AE		B	
LKGiW0001BHZA	2- 2	AS		B	
LKGiW7330BHZZ	4- 20	AY		B	
LKGiW7375BHZA	11-107	BH		S	
LPiN-6650BHZZ	4- 10	AA		C	
LPLTM6705BHZZ	2- 17	AX		C	
LPLTM6708BHZZ	4- 36	BB		C	
LPLTM6709BHZZ	4- 2	AS		C	
LPLTP6710BHZZ	4- 9	AK		C	
LPLTP6711BHZZ	4- 43	AP		C	
LPLTP6712BHZZ	4- 6	AK		C	
LX-BZ6444BHZZ	1- 62	AA		C	
"	1- 71	AA		C	
LX-BZ6775BHZZ	4- 29	AA		C	
LX-BZ6776BHZZ	4- 24	AA		C	
LX-BZ6778BHZZ	1- 33	AA		C	
"	4- 33	AA		C	
"	11- 4	AA		S	
LX-BZ6792BHZZ	1- 74	AF		C	
[M]					
MCAMM6633BHZA	4- 18	AE		C	
MLEVF6695BHZZ	4- 5	AK		C	
MSPRB6751BHZZ	4- 38	AF		C	
MSPRC6712BHZZ	4- 31	AF		C	
MSPRK6718BHZZ	4- 19	AF		C	
MSPRT6713BHZZ	4- 30	AD		C	
MSPRT6714BHZZ	4- 4	AE		C	
[N]					
NGERH2317BHZZ	3- 19	AR		C	
NRÖLP6650BHZZ	4- 13	AP		C	
"	4- 39	AP		C	
NRÖLP6651BHSC	1- 70	AE		C	
[P]					
PFiLD6973BHZZ	1- 49	AS		D	
PFiLW6961BHZZ	1- 6	AP		D	
PFiLW6976BHZZ	1- 1	AV		D	
PGiDH2394BHZZ	3- 20	AK		C	
PGUMM6695BHZZ	4- 32	AE		C	
PGUMM6725BHZZ	2- 15	AZ		C	
PGUMM6727BHZZ	4- 34	AE		C	
PRDAF6656BHZZ	5- 1	AK		C	
PRDAF6666BHZA	1- 39	AN		C	
"	7- 2	AN		C	
PRNGT6637BHZZ	4- 22	AA		C	
PRNGT6641BHZZ	11-108	AE		S	
PSHEP6681BHZZ	3- 2	AF		C	
PSHEP6854BHZZ	2- 16	BD		C	
PSKR-6628BHZZ	4- 8	AG		C	
[Q]					
QACCE3120BHZZ	1- 27	AV		B	
QACCL1018BHZZ	1- 27	AU		B	
QCNCM1060AC03	6- 1	AB		C	
QCNCM1101BHZZ	7- 3	AC		C	
QCNCM1101CCZZ	5- 2	AB		C	
QCNCM6865RC0B	11- 4	AA		S	
QCNCM7057RCZZ	5- 3	AB		C	
QCNCM7125BH01	6- 2	AN		C	
QCNCM7176BH01	6- 3	AD		C	
QCNCM7207BH4J	5- 4	AQ		C	
QCNCW1057ACZZ	6- 4	AB		C	
QCNCW2423BH0E	5- 5	AE		C	
QCNCW6882BH1A	5- 6	AG		C	
QCNCW7081BHZZ	5- 7	AB		C	
QCNCW7118BH01	5- 8	AG		C	
QCNCW7118BH1A	5- 9	AG		C	
QCNCW7201BH1E	5- 10	AK		C	
QCNCW7202BH1E	9- 1	AK		C	
QCNCW7242BH0B	7- 4	AD		C	
QCNCW7245BH1J	5- 11	AG		C	

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK	
QCNCW7246BH0H	5- 12	AG		C	
QCNW-1035CCZ1	1- 27	AN		B	
QCNW-3098BHZZ	5- 13	AP	N	C	
QCNW-3099BHZZ	5- 14	AN	N	C	
QCNW-7121RCZZ	1- 43	AD		C	
QCNW-7872BHZZ	1- 30	AK		C	
QCNW-7877BHZZ	8- 1	AN		C	
QCNW-7878BHZZ	1- 7	AK		C	
"	9- 2	AK		C	
QCNW-7880BHZZ	1- 19	AF		C	
QCNW-7881BHZZ	2- 3	AG		C	
QCNW-7886BHZZ	7- 6	AG		C	
QCNW-7889BHZZ	5- 15	AG		C	
QCNW-7890BHZZ	6- 5	AF		C	
QCNW-7895BHZZ	11- 4	AF		S	
QCNW-7898BHZZ	1- 76	AP		C	
QCNW-7915BHZZ	7- 5	AL		C	
QFS-A1037CCZZ	5- 16	AC		A	
QFS-C2521TAZZ	7- 7	AE		A	
QFS-C4301CCZZ	5- 17	AE		A	
QFSDH2109AFZZ	5- 18	AC		C	
"	7- 8	AC		C	
QPLGA0006QCZZ	1- 27	AQ		B	
QSOCZ2042SC32	5- 19	AE		C	
QSW-M6872BHZZ	4- 25	AR		B	
QTANZ6661BHZZ	1- 35	AE		C	
[R]					
RALMB6646RCZZ	5- 20	AN		B	
RC-EZ336ARC1A	5- 21	AB		C	
RCILC6647RCZZ	5- 22	AE		C	
RCILC6653BHZZ	7- 9	AS		C	
RCORF6696BHZZ	1- 40	AL		C	
RCORF6698BHZZ	1- 73	AR		C	
RCORF6699BHZZ	3- 15	AU		C	
RCORF6702BHZZ	5- 23	AF		C	
RCORF7002BHZZ	5- 24	AE		C	
RCRSP6664RCZZ	5- 25	AF		B	
RCRSP6676RCZZ	5- 26	AG		B	
RCRSZ6644RCZZ	5- 27	AD		B	
RCRSZ6662RCZZ	5- 28	AE		B	
RTRNP6898BHZZ	1- 29	BK		B	
RTRNP9524BHZZ	1- 29	BK		B	
[S]					
SPAKA8375BHZZ	4- 41	AD		D	
SPAKA8421BHZZ	3- 3	AX		D	
SPAKA8422BHZA	3- 1	AX		D	
SPAKC8420BHSB	3- 4	AY	N	D	
SSAKH0013HCZZ	3- 6	AA		D	
SSAKH3012CCZZ	3- 10	AA		D	
SSAKH3015CCZZ	3- 6	AA		D	
SSAKH4231CCZZ	3- 5	AA		D	
[T]					
TCADH6788BHZA	3- 13	AC		D	
TCADZ2001BHZA	3- 16	AM		D	
TGANE1001BHZC	3- 9	AG		D	
TINSE2433BHZZ	3- 7	BC	N	D	
TINSF2434BHZZ	3- 7	BC	N	D	
TINSG2435BHZZ	3- 7	BC	N	D	
TINSN7240BHZZ	3- 8	AF		D	
TINSS2436BHZZ	3- 7	BC	N	D	
TPAPR6645RC05	10- 1	AY		S	
[U]					
UBATZ6661RCZZ	1- 20	AZ		B	
UBNDA6630BHZZ	3- 18	AK		C	
UKOG-6634RCZZ	11- 12	AX		S	
UKOG-6705RCZZ	11- 11	BC		S	
UKOG-6725BHZZ	11- 13	BB		S	
[V]					
VCCCTV1HH101J	5- 29	AA		C	
VCCCTV1HH220J	5- 30	AA		C	
VCCCTV1HH221J	5- 31	AA		C	
VCCCTV1HH270J	5- 32	AC		C	
VCCCTV1HH331J	5- 33	AA		C	
VCCCTV1HH470J	5- 34	AA		C	
VCEAGA1CW106M	5- 35	AA		C	
VCEAGA1CW337M	5- 36	AB		C	
VCEAGA1CW476M	5- 37	AB		C	
VCEAGA1HW105M	5- 38	AB		C	
VCEAGA1HW106M	5- 39	AA		C	
VCEAGA1HW107M	5- 40	AA		C	
VCEAGA1HW226M	7- 10	AB		C	

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK	
VCEAGA1HW228M	5- 41	AB		C	
"	7- 11	AB		C	
VCEAGD1CW108M	5- 42	AE		C	
VCEAGU1HW338M	7- 12	AT		C	
VCEAGU2AW106M	5- 43	AB		C	
VCKYTV1HB102K	5- 44	AA		C	
VCKYTV1HB103K	5- 45	AB		C	
VCKYTV1HB222K	5- 46	AA		C	
VCKYTV1HF104Z	5- 47	AA		C	
VCQYN1HM333K	7- 13	AA		C	
VHD1SR1544001	5- 48	AB		B	
VHD1SS353// -1	5- 49	AB		B	
VHDCP301// -1	7- 14	AL		B	
VHDPS156// -1	7- 15	AE		B	
VHDSFPL52V// -1	5- 50	AC		B	
VHEPTZ6 .2A/-1	5- 51	AH		B	
VHEUDZ5 .1B/-1	5- 52	AC		B	
VHi27040RBV1A	5- 53	BN		N	B
VHi4AC16// -1	5- 54	AK		B	
VHi5108CP7H-1	5- 55	AW		B	
VHi10393F-1	5- 56	AC		B	
VHiD780021505	5- 57	AT		B	
VHiF258024PC/	5- 58	AZ		B	
VHiG76C256F70	5- 59	BC		B	
VHiH641510810	5- 60	BA		B	
VHiKA34063A-1	5- 61	AP		B	
VHiKiA431F/-1	5- 62	AK		B	
VHiLM2574-ADJ	7- 16	AU		B	
VHiLZ9AH39/-1	5- 64	BA		B	
VHiLZ9FT18/-1	5- 65	AZ		B	
VHiMAX211CAi1	5- 66	AW		B	
VHiSN74HC00DR	5- 67	AG		B	
VHiTD62308F-1	5- 68	AH		B	
VHiTD62503P-1	5- 63	AG		B	
VHPHDSP5621-1	8- 2	AM		B	
"	9- 3	AM		B	
VHV i CPS0 .5/-1	5- 69	AF		B	
VRD-RC2EY100J	7- 17	AA		C	
VRD-RC2EY122G	7- 18	AA		C	
VRD-RC2EY183J	7- 19	AA		C	
VRD-RC2EY223G	7- 20	AA		C	
VRD-RC2EY270J	9- 4	AA		C	
VRD-RC2EY300J	8- 3	AA		C	
VRS-TS2AD000J	5- 70	AA		C	
VRS-TS2AD100J	5- 71	AA		C	
VRS-TS2AD101J	5- 72	AA		C	
VRS-TS2AD102F	5- 73	AA		C	
VRS-TS2AD102J	5- 74	AA		C	
VRS-TS2AD103J	5- 75	AA		C	
VRS-TS2AD104J	5- 76	AA		C	
VRS-TS2AD105J	5- 77	AA		C	
VRSTS2AD1151F	5-100	AA		C	
VRS-TS2AD123J	5- 78	AA		C	
VRSTS2AD1330F	5-101	AA		C	
VRS-TS2AD151J	5- 79	AA		C	
VRS-TS2AD153G	5- 80	AA		C	
VRS-TS2AD163F	5- 81	AA		C	
VRS-TS2AD181J	5- 82	AA		C	
VRS-TS2AD183F	5- 83	AA		C	
VRS-TS2AD203J	5- 84	AA		C	
VRS-TS2AD221J	5- 85	AA		C	
VRS-TS2AD222J	5- 86	AA		C	
VRS-TS2AD223J	5- 87	AA		C	
VRS-TS2AD241J	5- 88	AA		C	
VRS-TS2AD272J	5- 89	AA		C	
VRS-TS2AD331J	5- 90	AA		C	
VRS-TS2AD334J	5- 91	AA		C	
VRS-TS2AD362F	5- 92	AA		C	
VRS-TS2AD472J	5- 93	AA		C	
VRS-TS2AD473J	5- 94	AA		C	
VRS-TS2AD562J	5- 95	AA		C	
VRS-TS2AD563J	5- 96	AA		C	
VRS-TS2AD680F	5- 97	AA		C	
VRS-TS2AD822G	5- 98	AA		C	
VRS-TS2AD912G	5- 99	AA		C	
VS2SA1036KQRC	5-102	AB		B	
VS2SC2412K/-1	5-103	AB		B	
VS2SC4153// -1	5-104	AG		B	
VS2SJ328-Z/-1	5-105	AP		B	
VSKRC106S// -1	5-106	AD		B	
VSKTA1663// -1	5-107	AE		B	



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